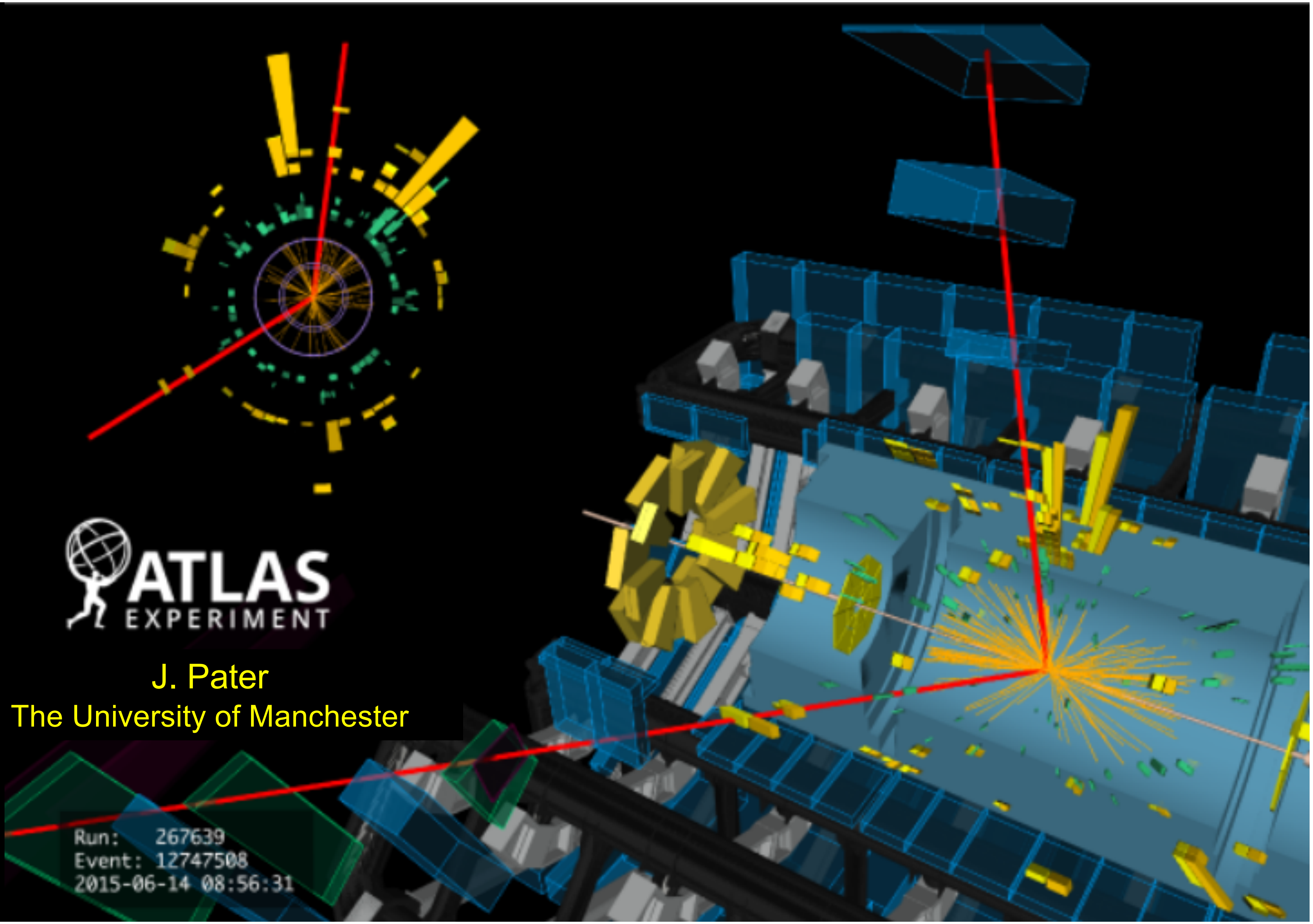
UK Contribution to the Phase-II upgrades of the ATLAS experiment for the luminosity frontier at the Large Hadron Collider

Universities of Birmingham, Cambridge, Edinburgh, Glasgow, Lancaster, Liverpool, Manchester, Oxford, Queen Mary UoL, Royal Holloway UoL, Sheffield, Sussex, UCL, Warwick, & STFC RAL



J. Pater
The University of Manchester

LHC physics – the priority for the community

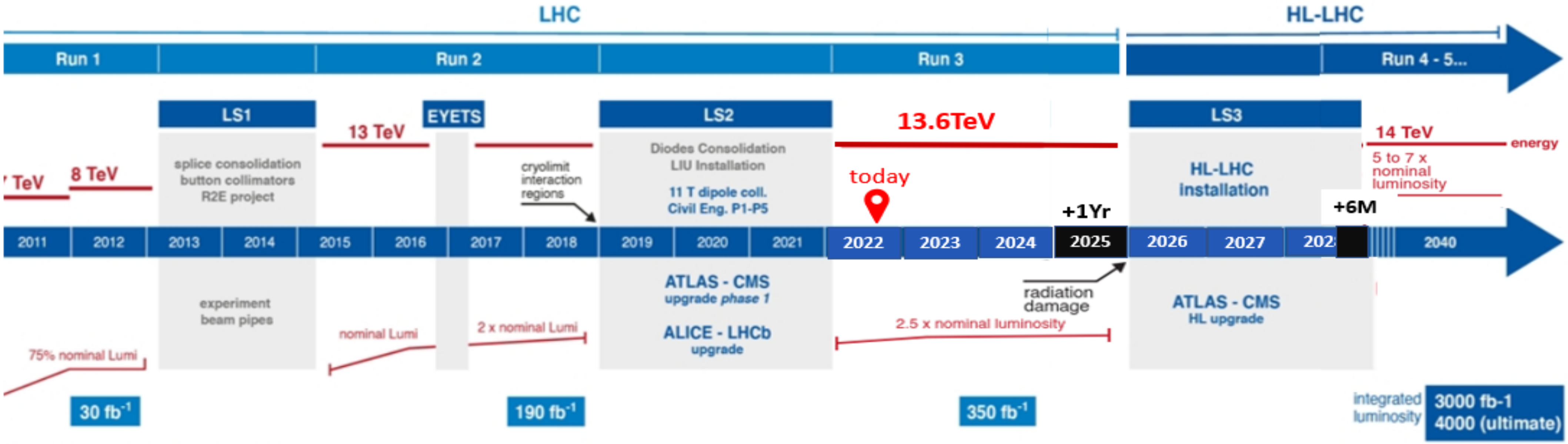
- The LHC defines the high-energy frontier in particle physics
  - It has done for the last 10 years and will do for the next 20 years.
- At end of Run-2, ATLAS had collected ~4% ($156fb^{-1}$) of the total data set we could expect at the end of Phase-II ($4ab^{-1}$)
  - The LHC has done a lot already and offers massive potential for the future.
- The LHC is a key part of both European and UK forward strategy:
  - **The 2020 European Strategy for Particle Physics concluded:**

    "The successful completion of the high-luminosity upgrade of the machine and detectors should remain the focal point of European particle physics, together with continued innovation in experimental techniques. The full physics potential of the LHC and the HL-LHC, including the study of flavor physics and the quark-gluon plasma, should be exploited."

  - **The UK Particle Physics Advisory Panel concluded:**

    "The HL-LHC remains the highest priority for the UK community, with direct involvement from a large fraction of the experimental community; this, coupled with the large investments so far, means that the UK must continue to give strong support to the ATLAS, CMS and LHCb upgrades, and their commissioning, and to the exploitation of the current and upgraded experiments, thereby maintaining its leadership in the LHC program."

HL-LHC Upgrade Timeline

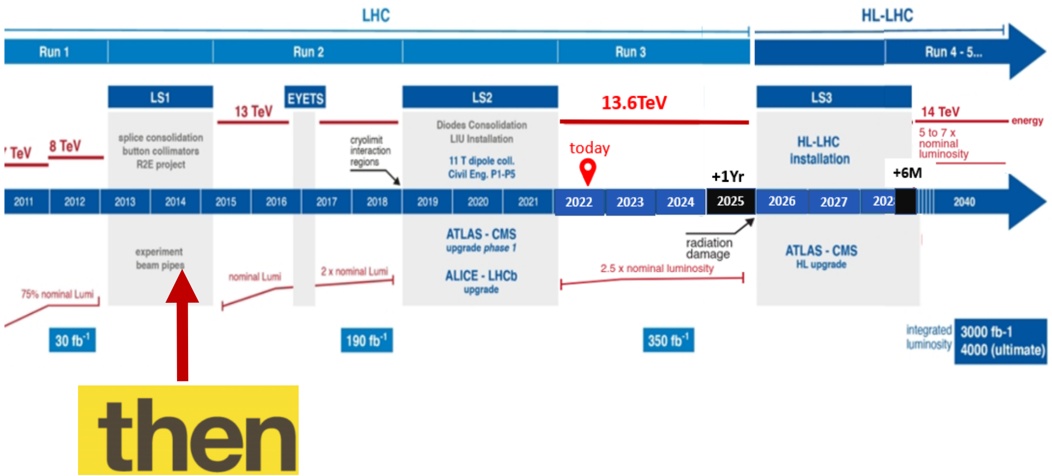


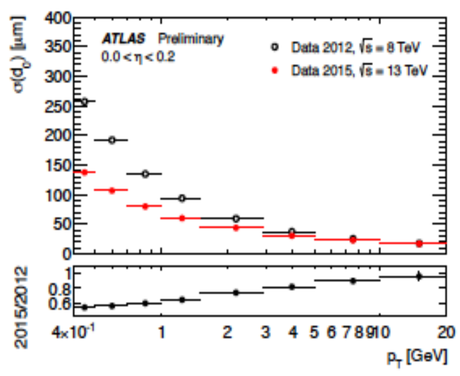
- Considerable progress to date:
  - 2012: Letter of Intent
  - 2015: Scoping Document
  - 2017-present: Seven Technical Design Reports
    - See backup slide
- CERN has recently increased the length of Run-3 to 4 years

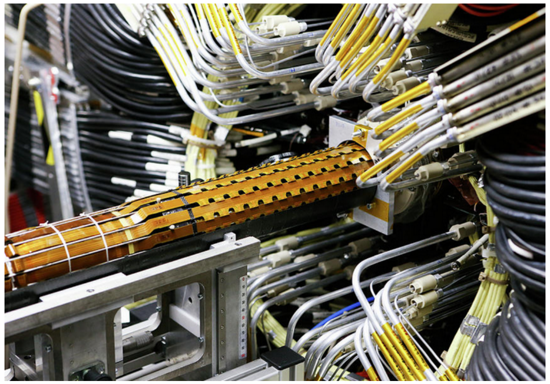
  … and extended the length of LS3 by 6 months, …

  … delaying the start of Phase-II by 18 months.

ATLAS Phase 0 – during LS1 : 2013-2014

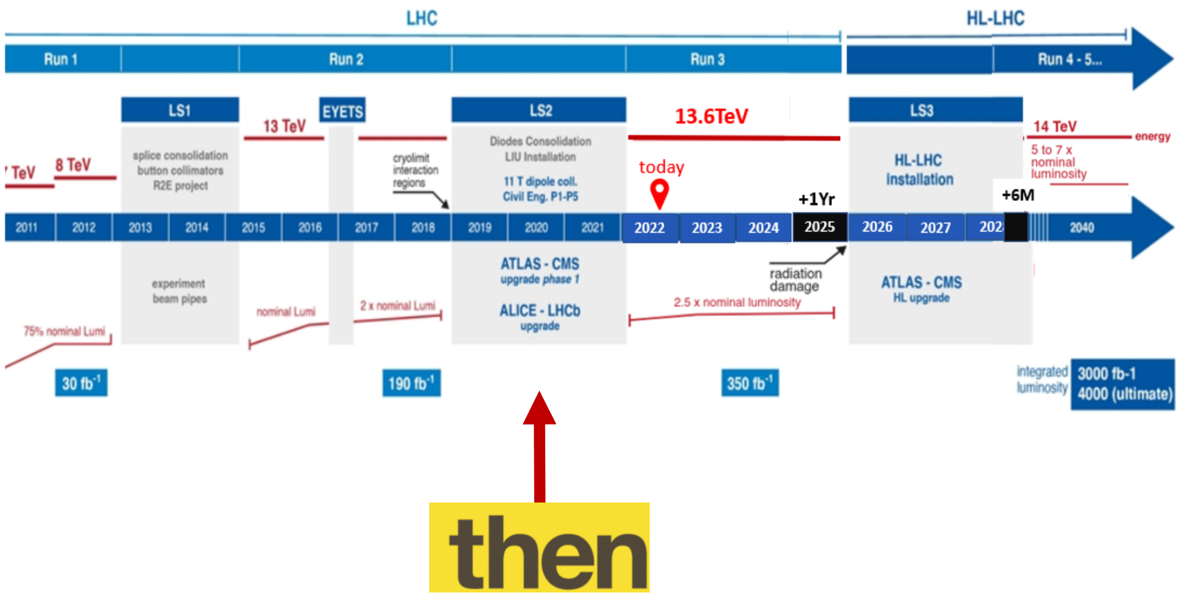






- Infrastructure:
  - New beam-pipe, improvements to magnet & cryogenic system
- Detector consolidation
  - Muon chamber installation complete(|η|=1.1-1.3) and repairs, improved readout of various systems (L1 rate increased to 100 kHz), repair of pixel modules and calorimeter electronics, new pixel services, new luminosity detectors, new MBTS detector
- 4^{th} silicon pixel detector layer (IBL)
  - Innermost Pixel detector layer at R=3.3 cm from beam
- Trigger & DAQ improvements
  - Topological L1 trigger, new Central Trigger Processor (CTP), coincidence between Tile and muons, restructuring of high-level trigger, new Fast TracK Trigger (FTK), improved L1 calorimeter trigger, upgrade ROS
- Software
  - Improvements to simulation, reconstruction, grid and analysis software
- Installation of Forward Proton Taggers Detectors (AFP)

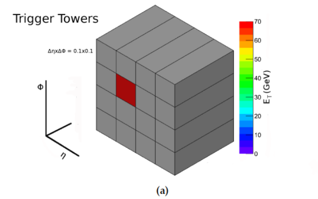
ATLAS Phase I – during LS2 : 2019-2020

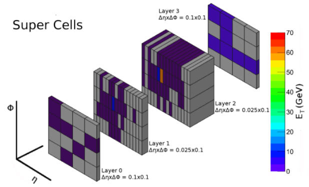


- Infrastructure improvements
  - Civil engineering P1 & P5
- Upgrade TDAQ
  - L1 Calorimeter trigger
    - See next slide
  - L1 Muon trigger
  - Topological triggers
  - High Level Trigger
  - Readout
- LAr readout electronics
- New Small muon Wheel
- Forward detector system
- Computing

Upgraded Calorimeter electronics– Phase I

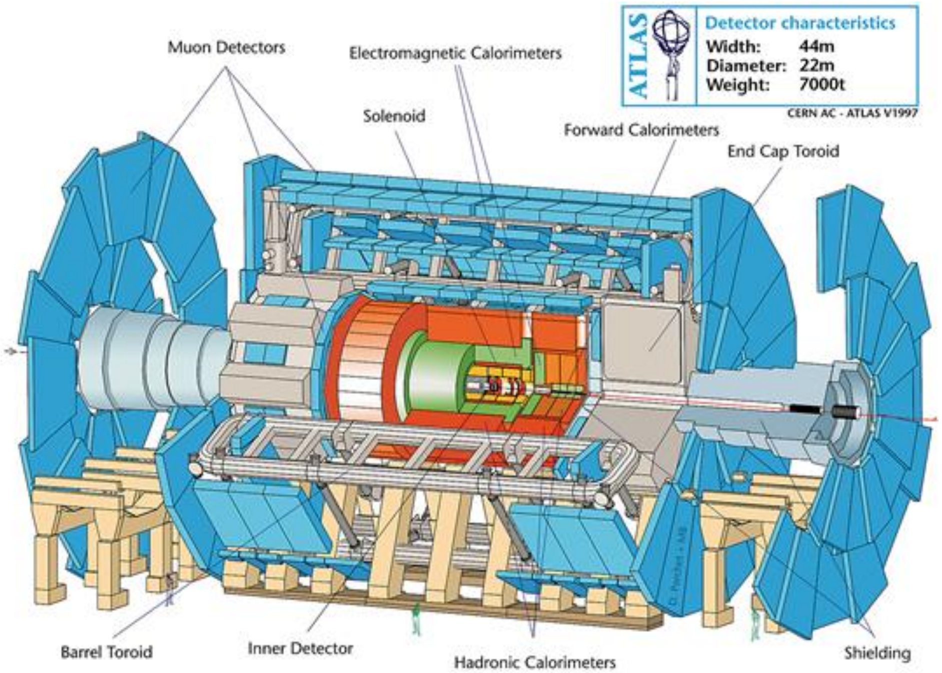
- ATLAS Liquid Argon Calorimeter
  - Increase in cell granularity
    - Original $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$
    - NewSuperCell $\Delta\eta \times \Delta\phi = 0.025 \times 0.1$
  - Improves
    - Energy resolution, efficiency for electrons, photons, tau leptons, jets and transverse missing energy.
  - L1 calorimeter feature extractors
    - eFEX, jFEX, gFEX, fFEX (not until phase II)
  - electron Feature Extractor eFEX
    - Hardware, firmware and software
    - Respond to new inputs and transmission, in presence of increased pile-up using existing latency
    - Integrate with neighbouring modules in the RO chain
    - Exploit improved granularity
    - Improved electron, photon, tau-hadron triggering
    - Improved isolation strategy
    - Output primitive objects for global trigger





eFEX in Crate in ATLAS Cavern

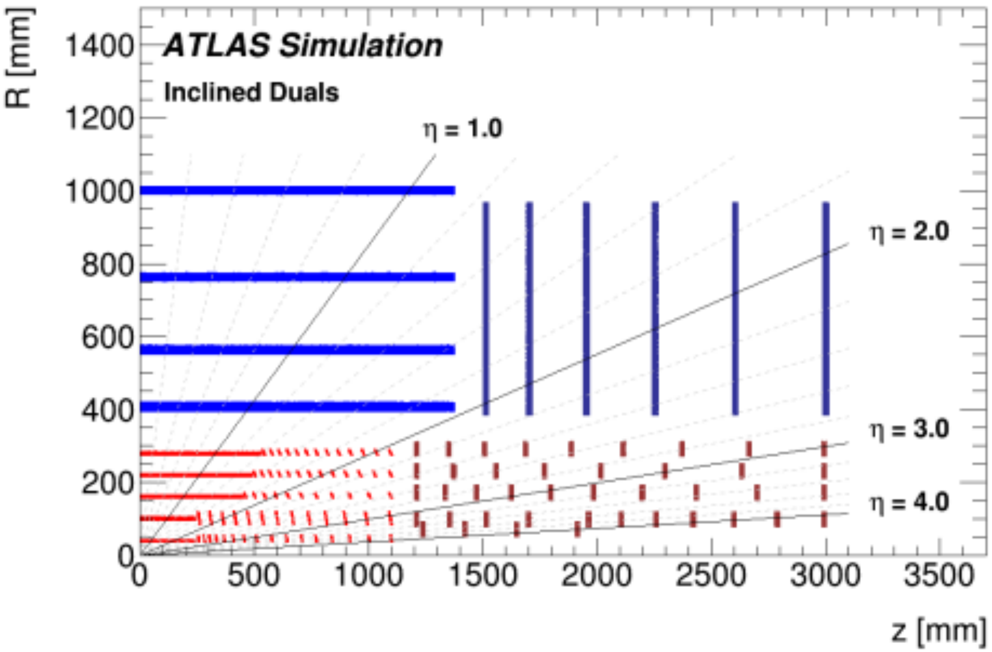
ATLAS - Upgrades - Phase 2



- All-new Inner Tracking Detector ITk
  - Strips and Pixels
- Muon system upgrade.
- Upgrades to the LAr & Tile Calorimeters
  - and associated Triggering
- Upgraded TDAQ System
  - DAQ
  - Event triggering & filtering,
- Computing
  - Offline software
  - Simulation & reconstruction
- High Granularity Timing Detector HGTD

Red font signifies UK participation

Upgraded Tracker ("ITk"): General Design Considerations



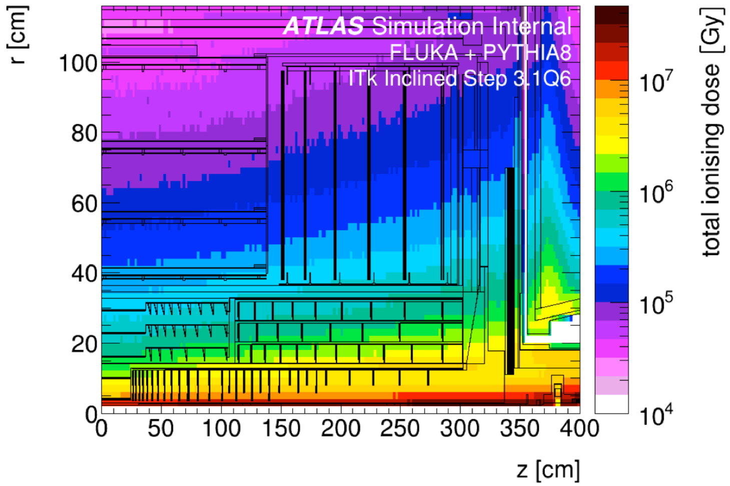
- Total Integrated luminosity up to 4,000 fb^{-1}
  Inner Pixel section replaced after 2,000 fb^{-1}
- Instantaneous luminosity up to 7.5 x 10^{34} cm^{-2} s^{-1}
  200 inelastic proton-proton collisions per crossing
- More than 10 years of operational lifetime

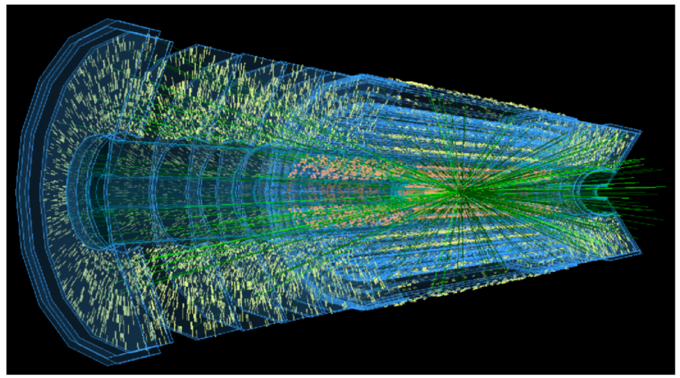
- Replaces the existing Inner Detector (ID) with an all-silicon design
  - ID Components >20 years old
  - Approaching radiation lifetime
- ITk Design based on ~10 years of operation with ID:
  - Monolithic all-silicon design
  - 5 barrel pixel layers & forward disks to $|\eta| = 4$
  - 4 barrel strip layers & 6 end cap discs on each side
- Designed for
  - low mass, high tracking efficiency, low fake rake
  - tracks $P_T > 1$ GeV, primary & secondary VTX reco
  - fault tolerant against limited component losses
  - accommodate timing detector at high η
  - 1 MHz readout L0 Only, 4 MHz L0-L1
- Re-using many existing services: HV, LV cable & gas
- New CO_2 cooling

2017 The Strip tracker Technical Design Report
https://cds.cern.ch/record/2257755/files/ATLAS-TDR-025.pdf
2018 The Pixel tracker Technical Design Report
https://cds.cern.ch/record/2285585/files/ATLAS-TDR-030.pdf

More technical challenges for ITk

- Unprecedented requirements on radiation tolerance
  - As high as 10 MGy total ionising dose
- Unprecedented requirements on cooling
  - 300kW of $C0_2$ cooling for ITk & HGTD
- Driven to low power on-detector, small feature sizes, novel powering (DC-DC or SP), services.
- ID End-of-life issues
  - Decommissioning, replacement
- High Trigger rates and data volumes:
  - readout complexity
  - pattern recognition, simulation and reconstruction challenges



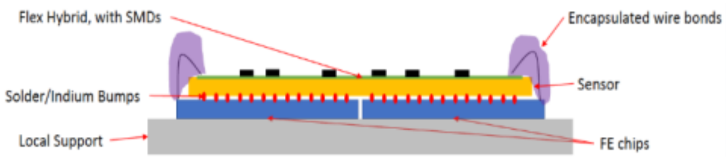


https://twiki.cern.ch/twiki/bin/view/AtlasPublic/UpgradeEventDisplays

Strips & Pixels, UK Involvement

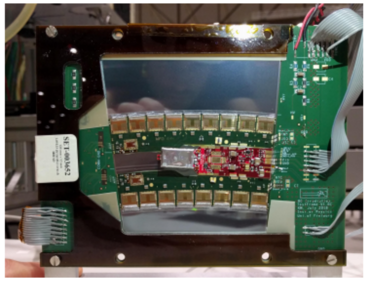
• PIXELS

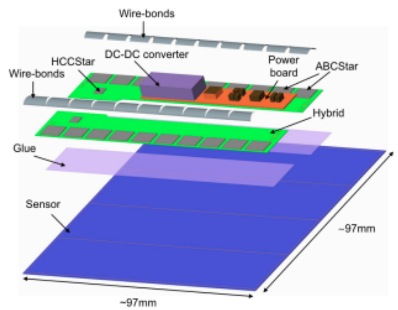
- Active area of 12.7 m² of silicon
- > 10,000 installed modules
- Pixel size 50 x 50 μm^2 or 25 x 100 μm^2
- Sensors
  - **Layer 0**: thin edge 3D sensors, radius 39mm up to 1.3 x 10^{16} n_{eq}/cm^2
  - **Layer 1**: 100 μm planar n-in-p technology
  - **Layers 2, 3 & 4**: 150μm to 4,000fb^{-1}
  - Multiple vendors, choices based on performance, cost & capacity
- FE Readout
  - Realized in 65 nm TSMC technology, Chip size ~2x2cm²
    with 160k pixels. 4 x 1.28 Gb/s links with data compression. Occupancy up to 223 hits/chip/BC
  - Demonstrator chip based in RD53A
  - Serial powering, module assembly and performance



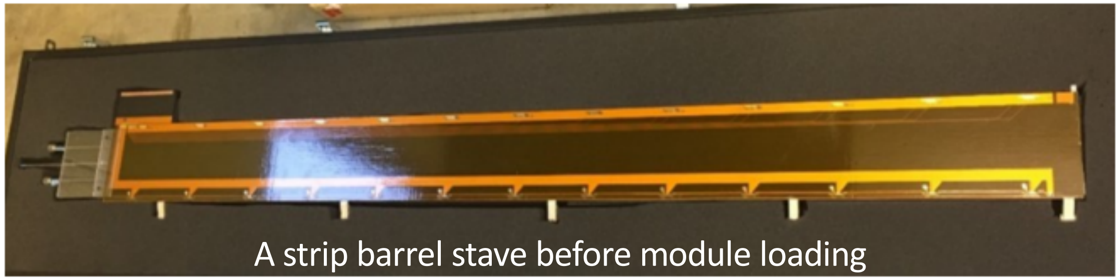
• STRIPS

- Active area of 165 m² of silicon
- 17,888 installed modules
- Strip pitch ~70μm, > 59 M channels
- Highly modular, designed for ease of construction
- Global construction
- Modules ~10cm² (1 sensor/module)
- Short (long) strips in barrel close to (far from) IP
- Sensor vendor HKP – contracts now signed
- FE Readout
  - GF 130nm technology, 640 MB/s

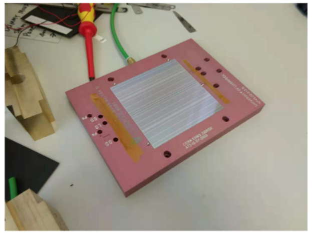


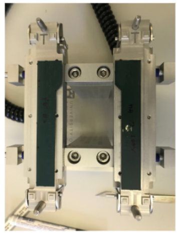


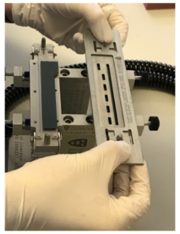
ITk Strip Hardware developments

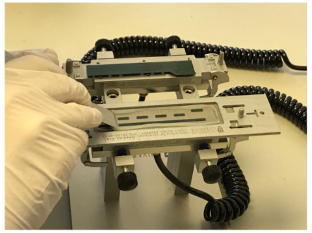


A strip barrel stave before module loading

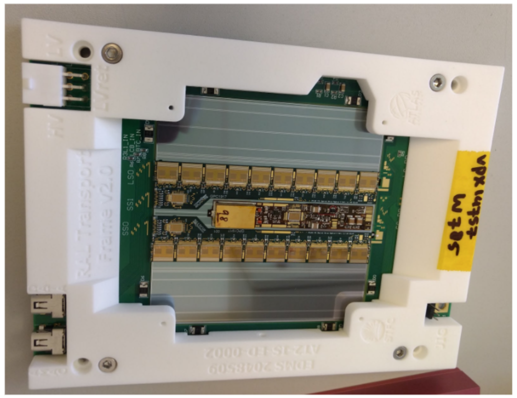




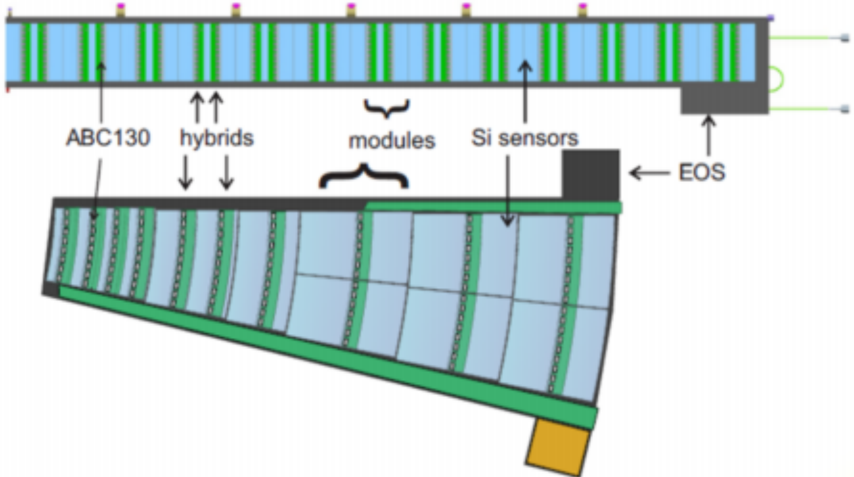


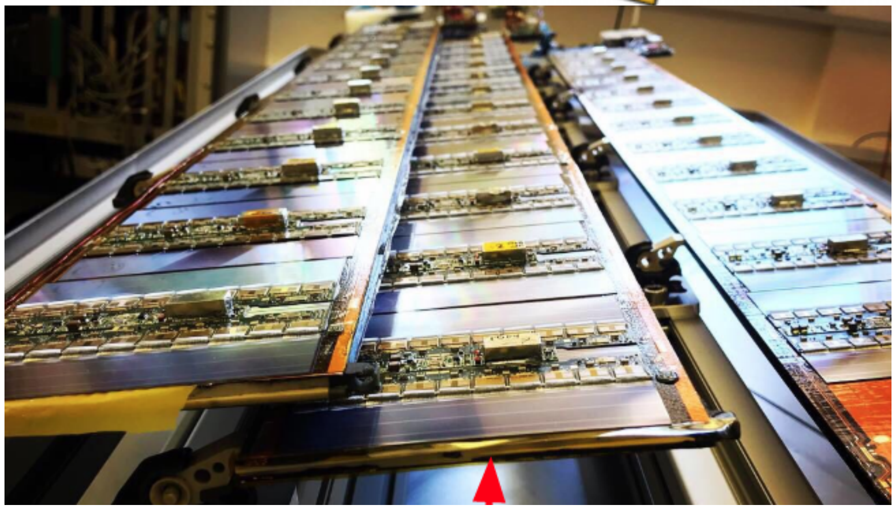


Short Strip Module

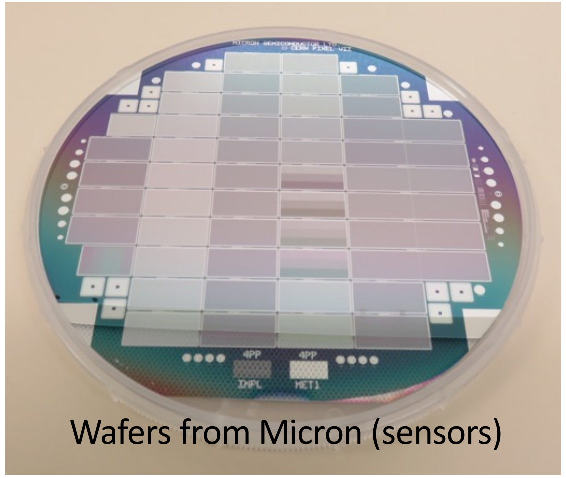


Long Strip Module



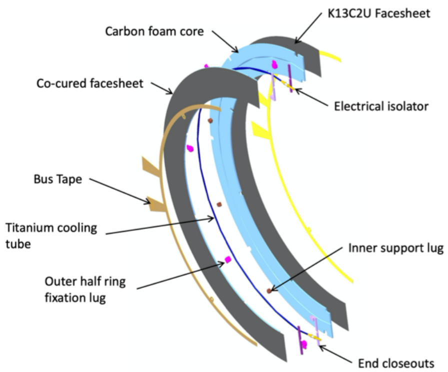


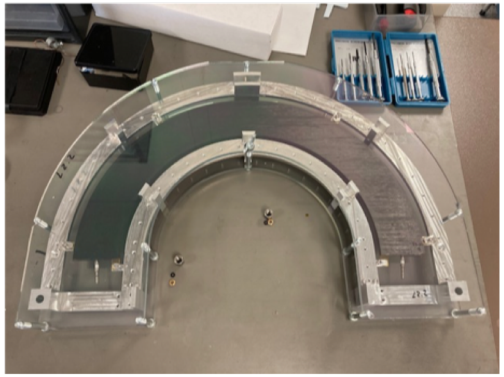
ITk Pixel Hardware developments

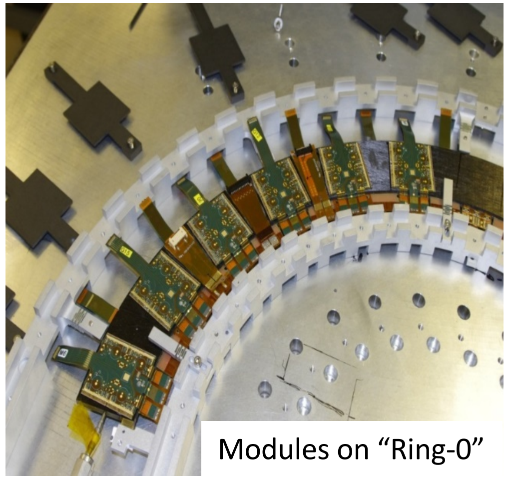


Wafers from Micron (sensors)

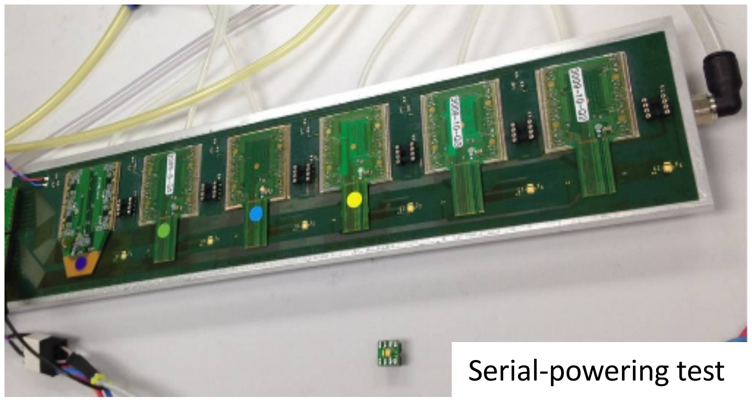
UK will deliver one Pixel End-Cap



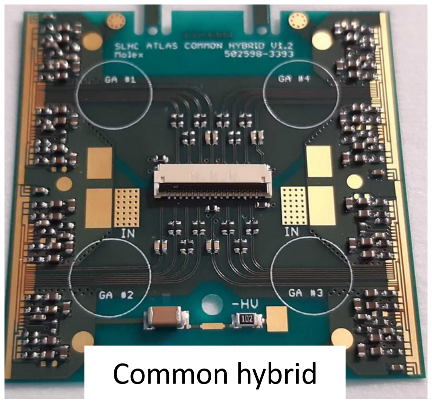




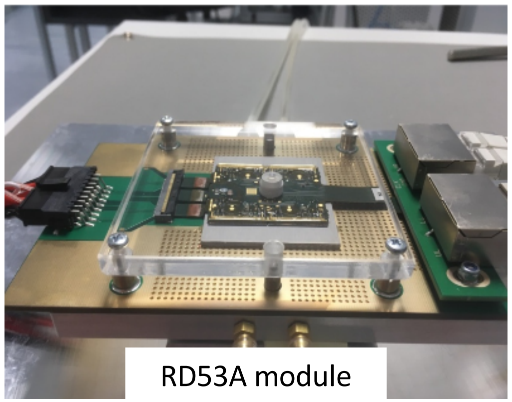
Modules on “Ring-0”



Serial-powering test



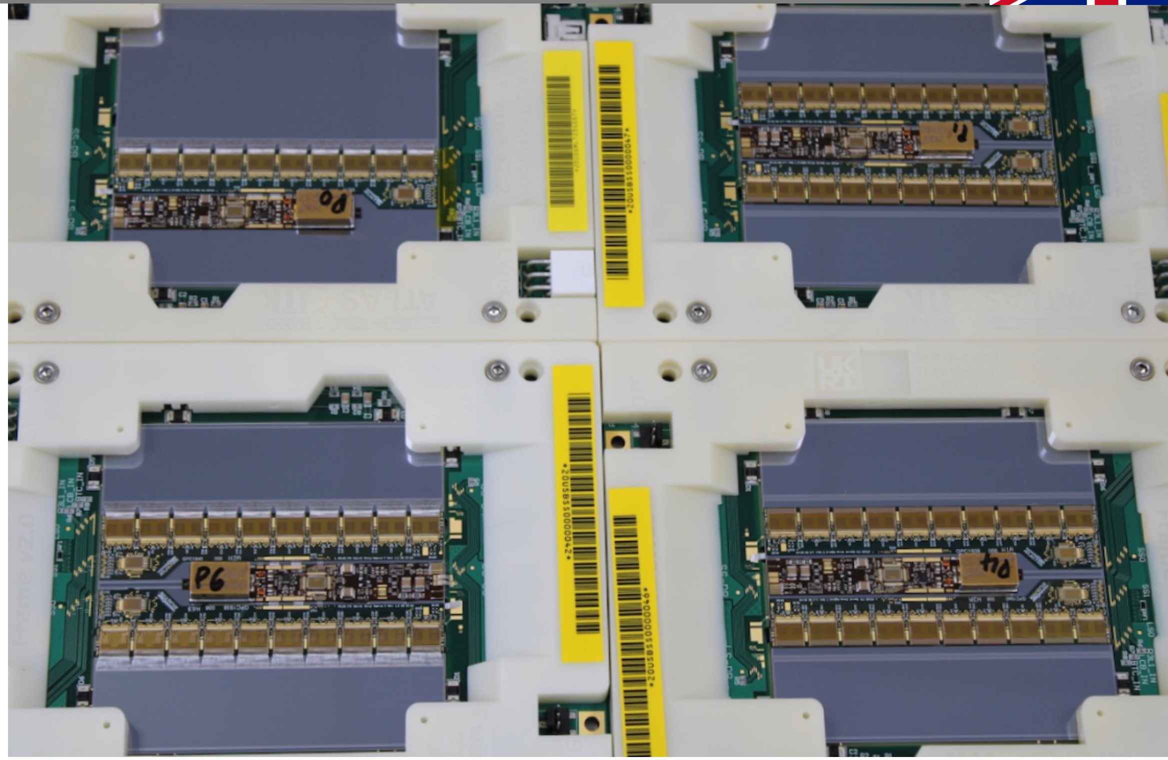
Common hybrid



RD53A module

Half-cylinder manufacture

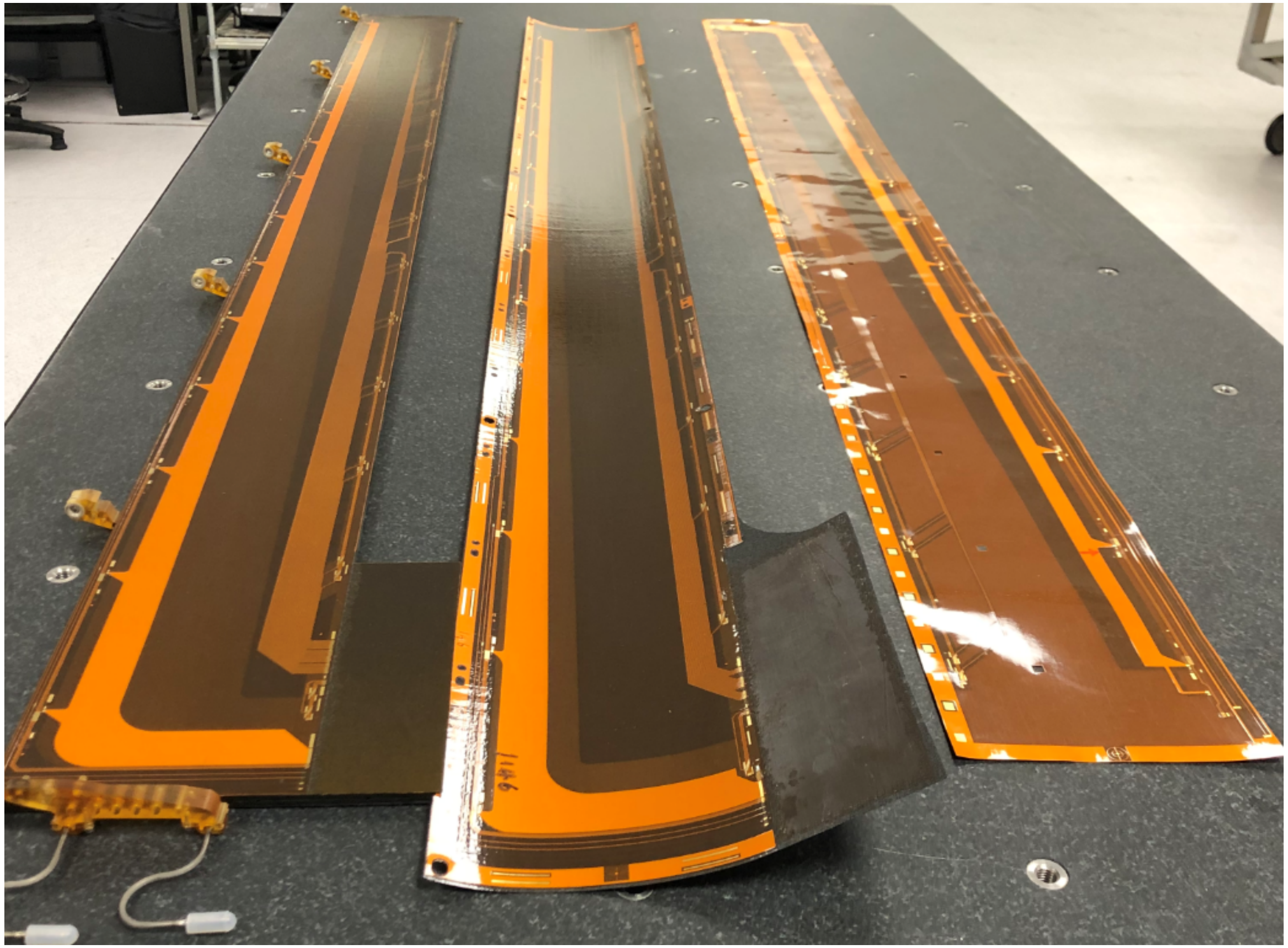
What's happening now: WP12 Strip Modules



one of the 12 GaNFET wafers that were delivered to the UK, passed QC in UK and then sent on to LBNL & Freiburg

Four pre-production modules in various states of assembly: 1 long-strip module and 3 short-strip modules. These have now been mounted on a pre-production stave.

What's happening now: WP14 Strip Stave Cores



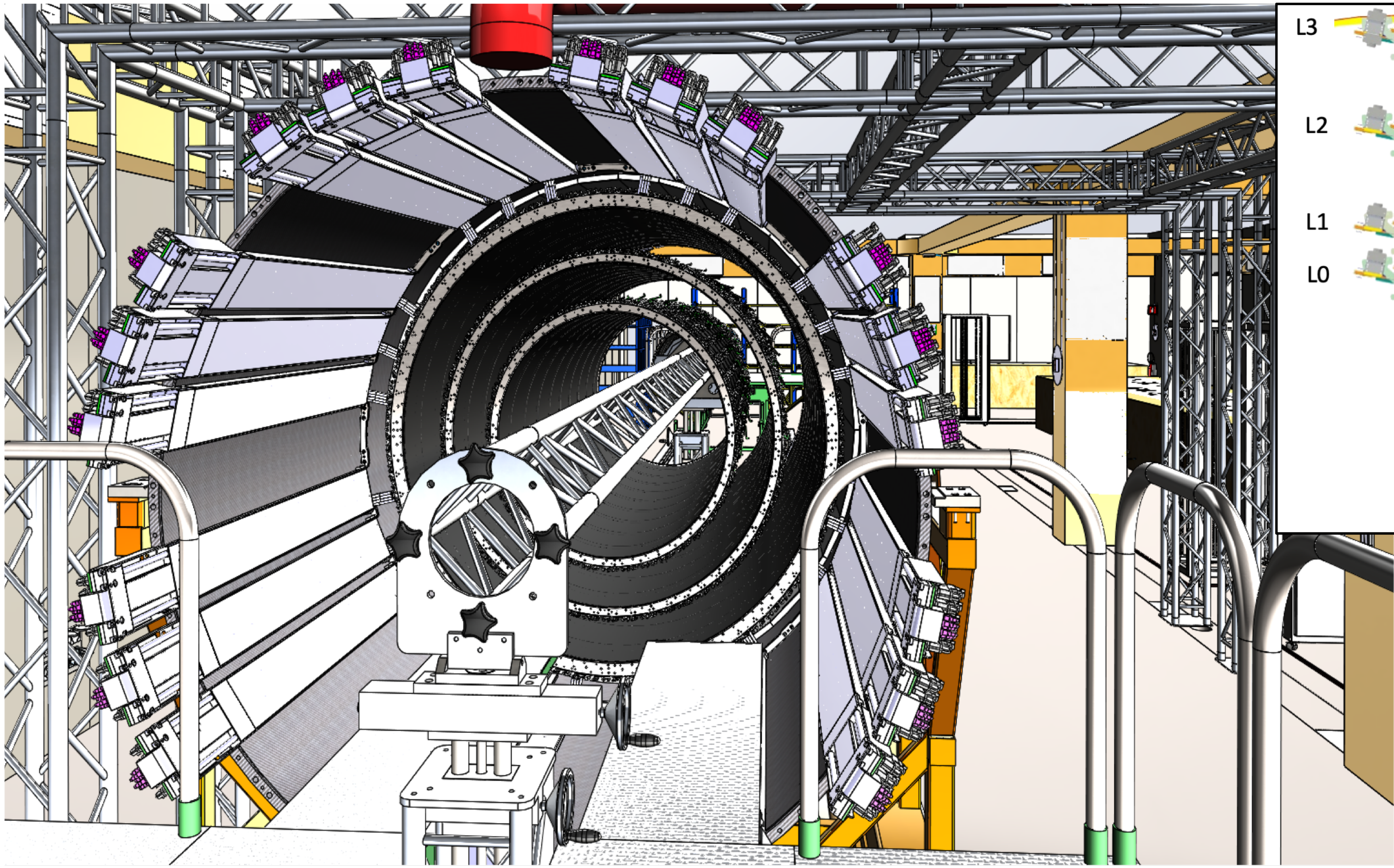
From right to left:

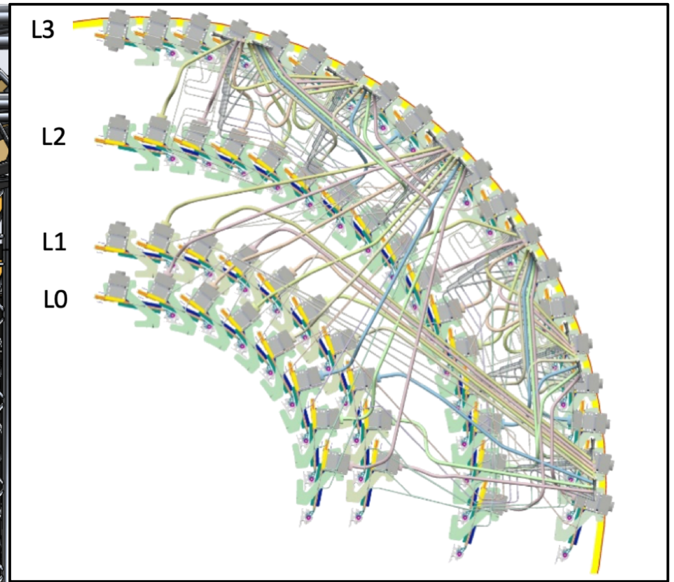
- Bare Cu/polyimide stave bus tape
- Co-cured tape (i.e. connected to carbon fibre skin) You can see the carbon fibre in the "ear" which is where EOS PCBs will be mounted.
- Completed barrel stave: showing top co-cure, cooling loop inlet and outlet and lock points for mounting on barrel with brackets.

What's happening now: WP15, WP18

WP15: Strip Stave Assembly and Loading (left photo)
WP18: Strips DAQ, Readout, testing. Right photo: operation of a Strip Barrel Stave

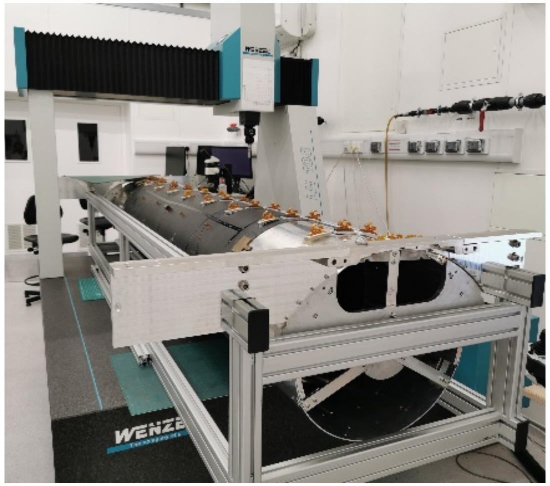
What's happening now: WP17 Strips Integration

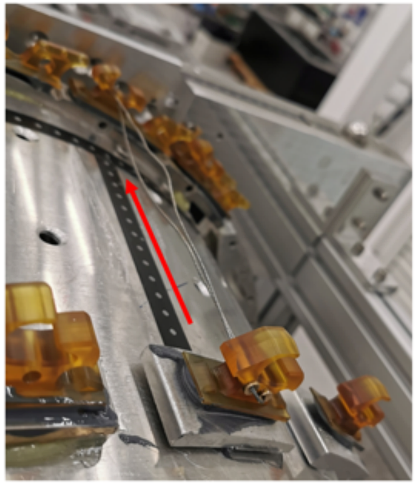


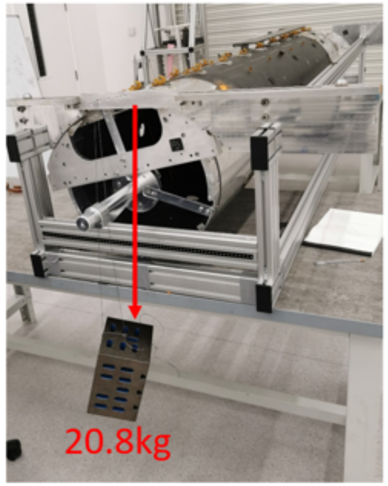


Strips Integration: Design

What's happening now: WP17 Strips Integration





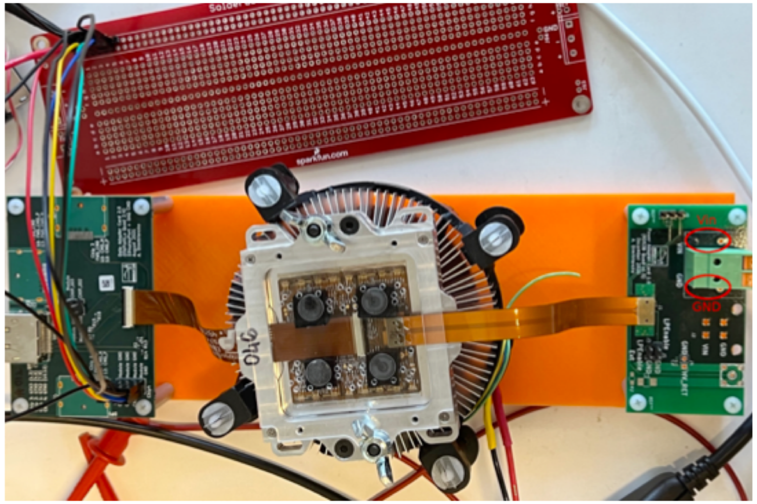


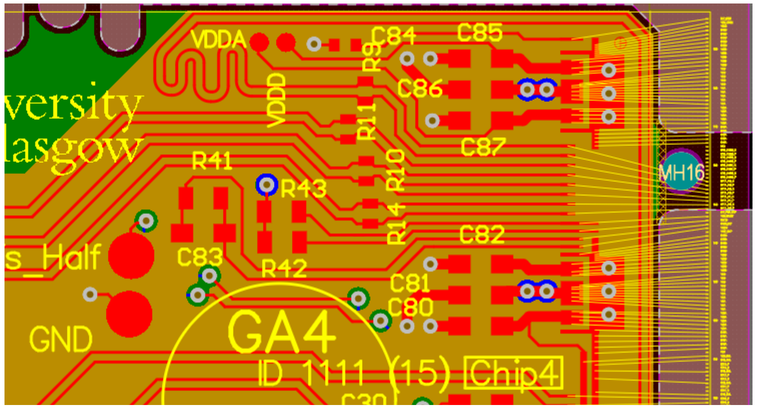
A complete set of tooling for Strip cylinder dressing is available.

- The prototype cylinder that is used to validate the dressing tooling and gluing procedures has been configured to have the correct geometry and allows 3 rows of brackets to be glued.
- Several trial stave insertion runs have been made with the prototype cylinder.
- CMM surveys of brackets' positions made for all trials.

Strips Integration: Realisation

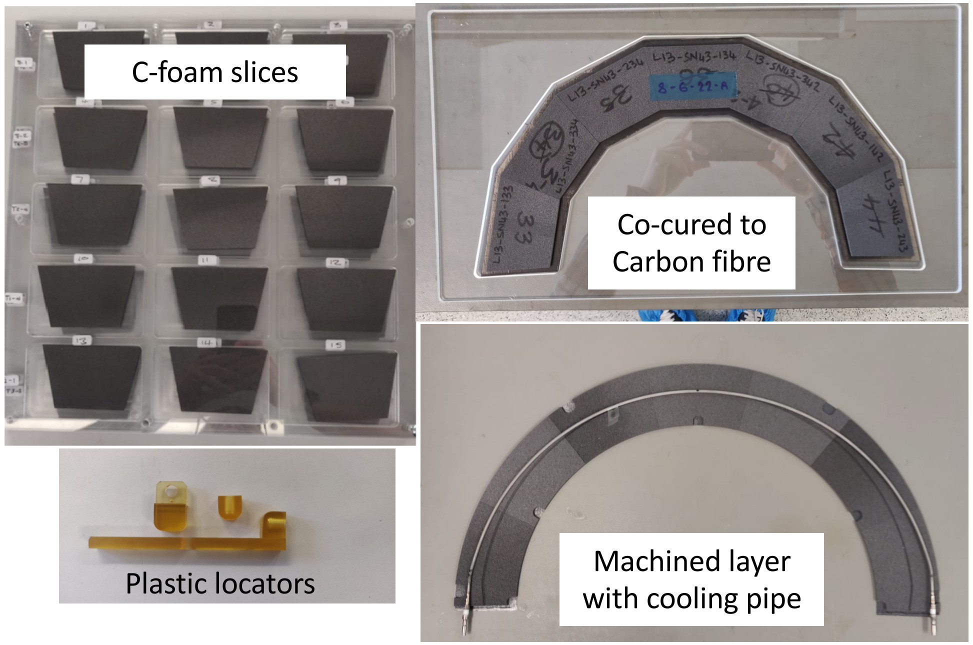
What’s happening now: WP13 Pixel Modules

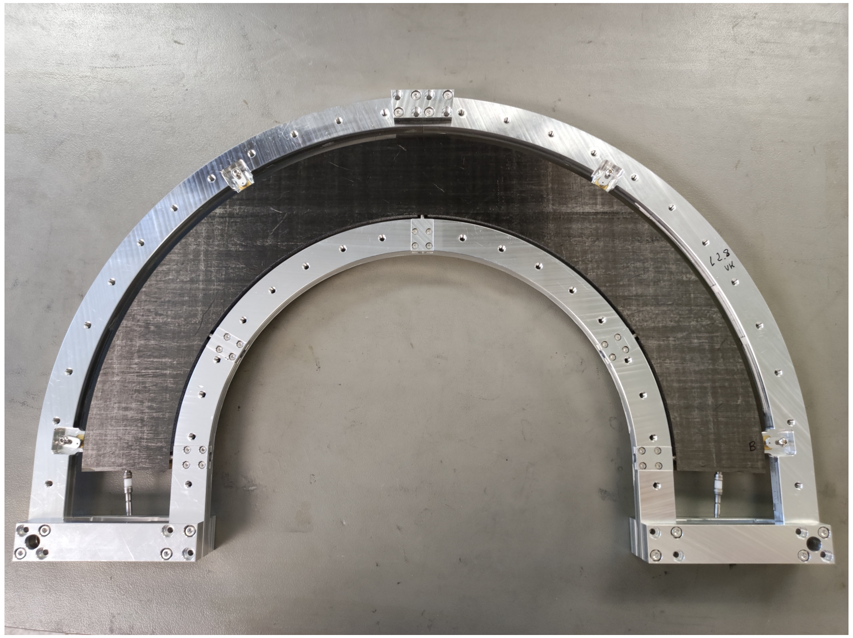




- Much prototype work done with RD53A-based modules
  - (RD53A = pre-prototype readot ASIC)
  - Module assembly, quality control, loading onto half-rings, …
  - Final Design Review passed earlier this year
- Now moving to Itkpix-1
  - 1st version of final chip
  - Some prototypes in hand now, have led to minor flex-hybrid design changes
- Hopefully-final hybrid design now complete
  - Pre-production flex order proceeding
  - Expect delivery in December

What's happening now: WP16 Pixel half-rings

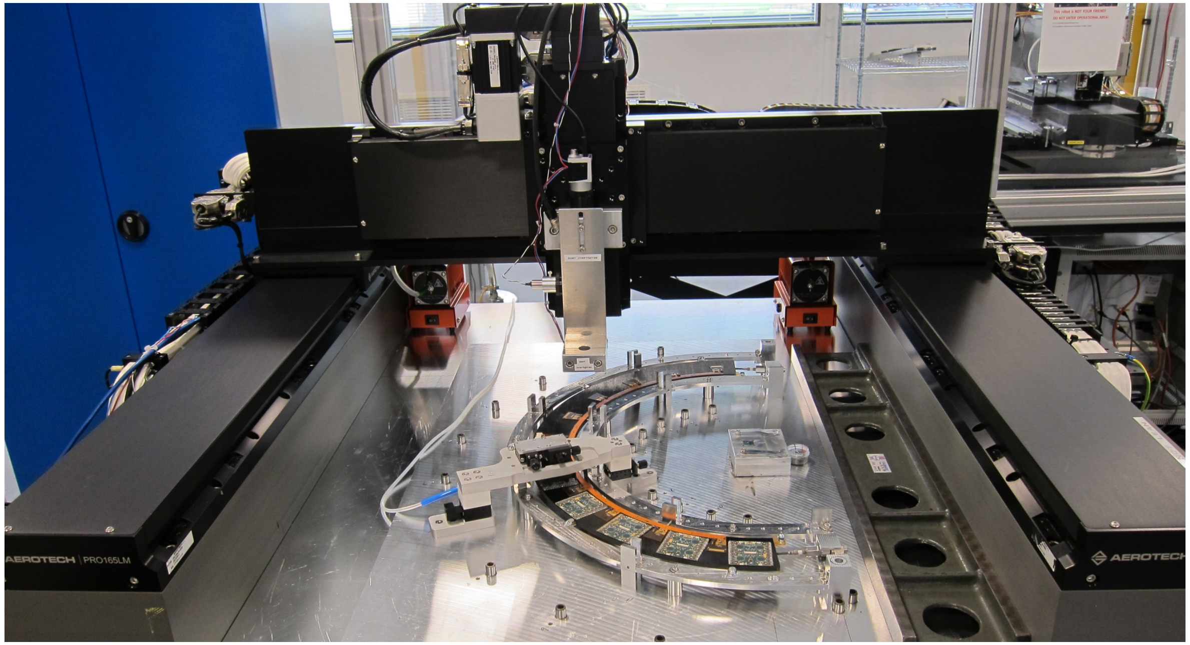




- Carbon-based half-rings hold single rows of modules
- Shown: components and steps in half-ring production

- Currently in pre-production:
  - 2 of 2 Layer-2 half-rings produced
  - 1 of 2 Layer-3 half-rings produced
  - Production Readiness review in January

What’s happening now: WP19 Pixel loading



Here, pixel modules are loaded on to Pixel half rings using a bespoke gantry system.

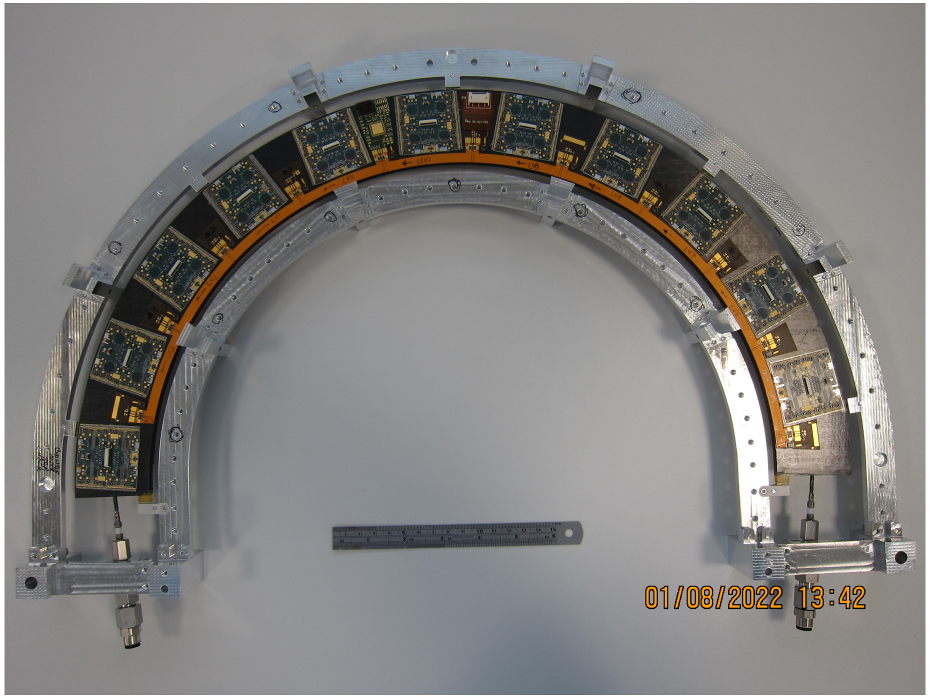
The exact locations are constrained…

… and knowledge of where the modules are placed is important.

Here we see Half Ring Metrology.

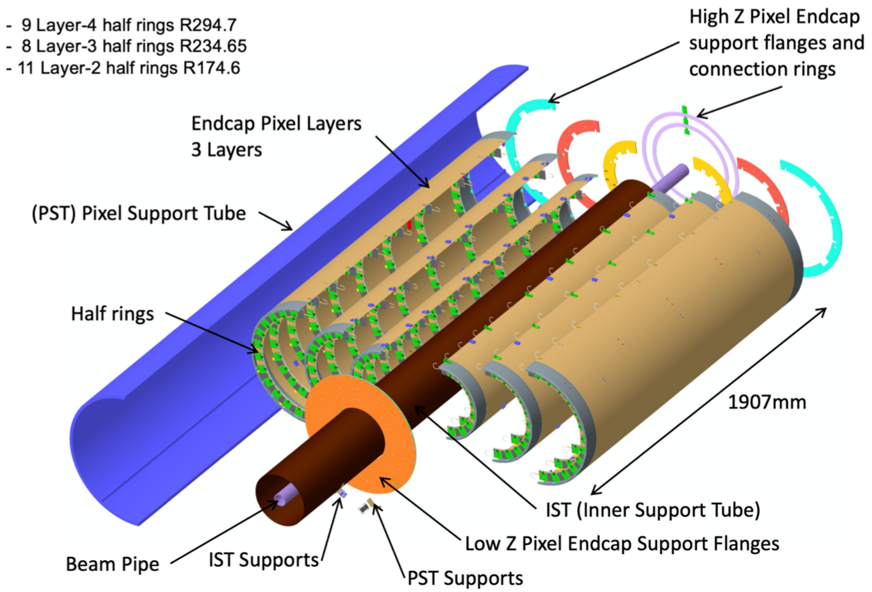
What’s happening now: WP19, continued

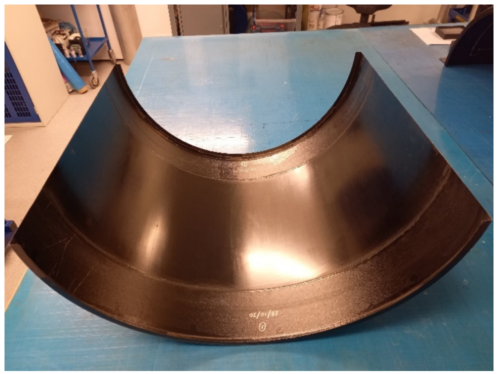
A few of the UK team with a Pixel half-ring prototype loaded with silicon heaters for thermal qualification of the bare local support structure.

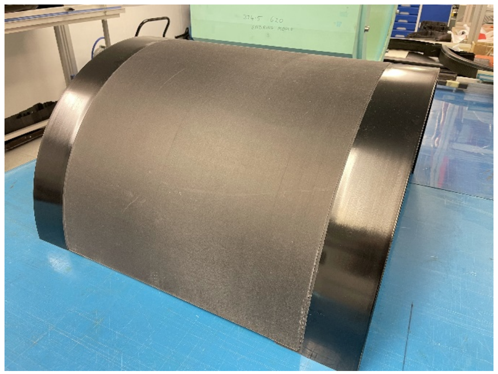


A Pixel half-ring fully loaded with working demonstrator (RD53A) modules, now undergoing electrical system testing.

What's happening now: WP20 Pixel Integration

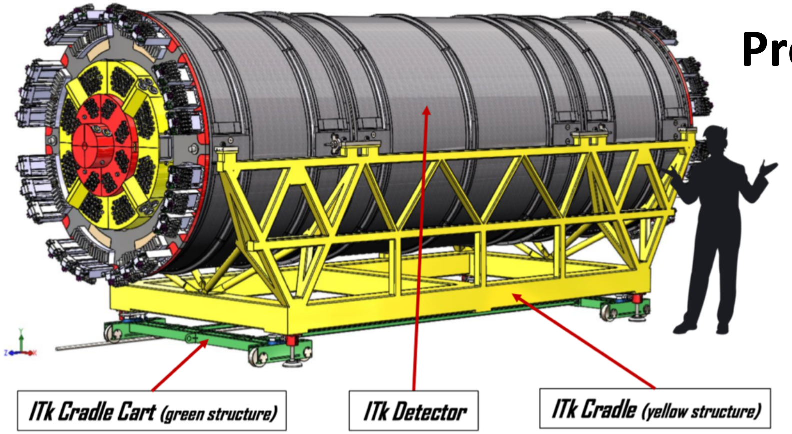




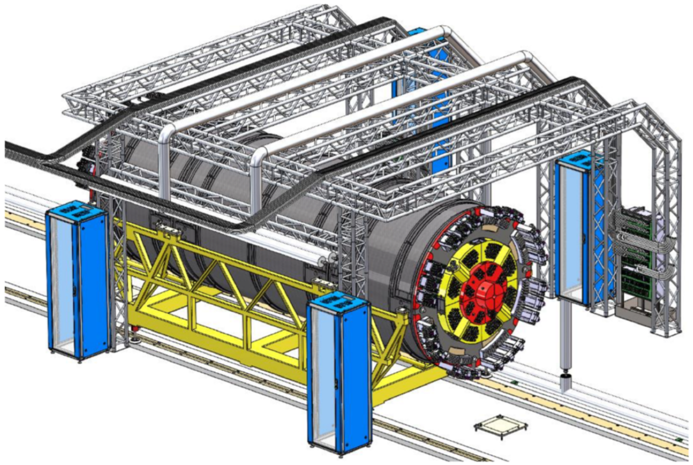


Prototyping pixel global supports

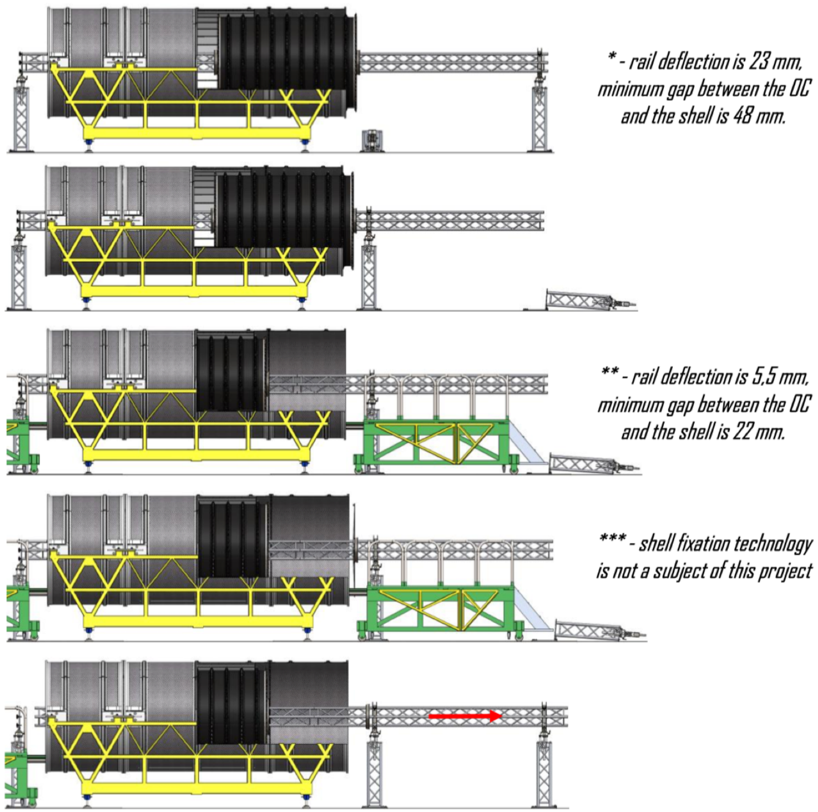
What's happening now: WP21 (recent bid)



Preparation for ITK Integration & Commissioning at CERN



Service cages (services routing & support structures)



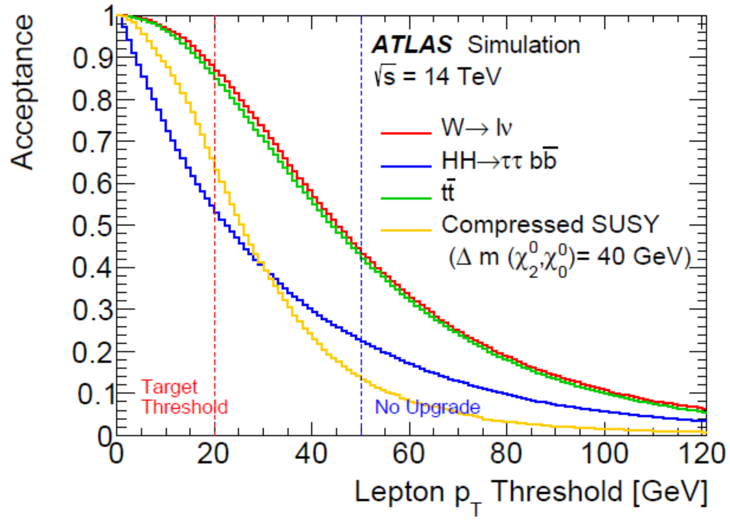
Cylinder insertion sequence

TDAQ upgrade - Physics Motivation

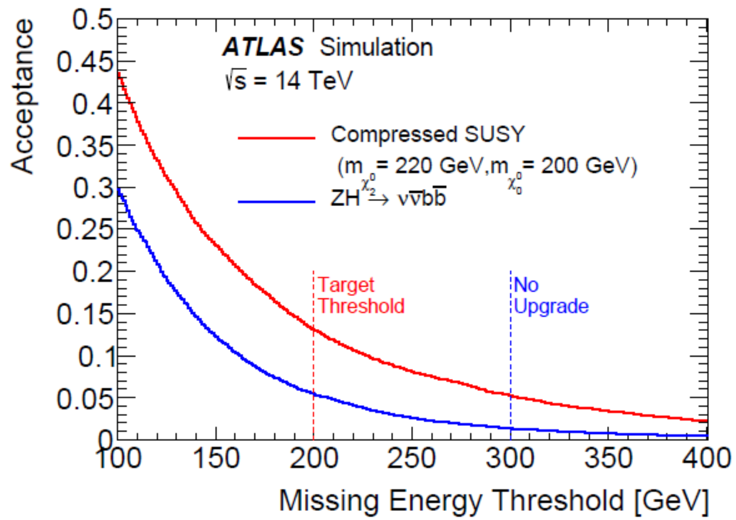
CERN-LHCC-2017-020

Physics searches require keeping the p_T of the various trigger objects as low as possible:
- Electroweak scale requires low p_T leptons
- Searches for new physics
- HH measurements requires low p_T jets/b-jets

Signatures with Single-Electron & Single-Muon Triggers



Signatures with Missing Transverse Energy



TDAQ in Phase-II – Original Plan

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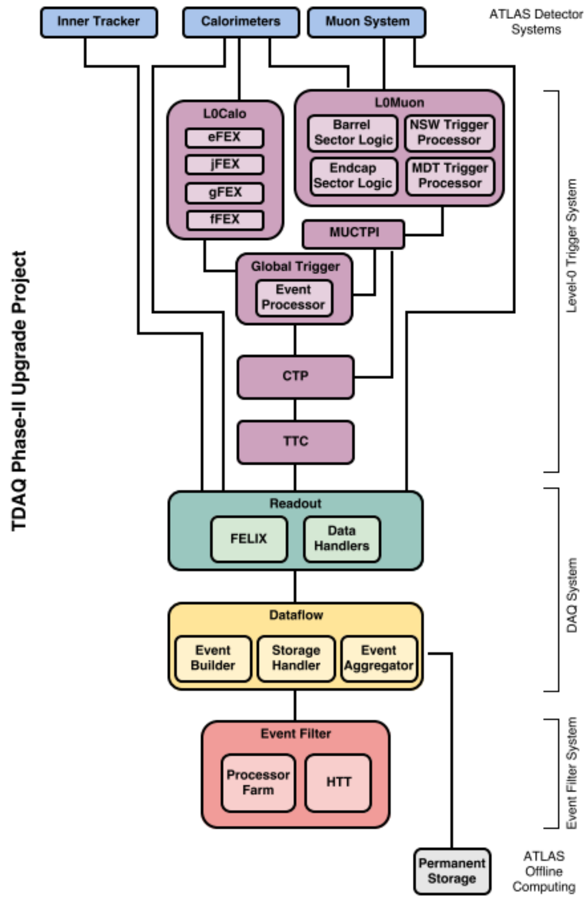
- Baseline is a single-level of Hardware trigger L0 with output rate at 1 MHz (latency/rate < 10 μs)
- Input from Calorimeter and Muons
- Hardware Track Triggering.
  - Provides for the event filter, regional tracking guided by L0 at an output rate of up to 1MHz (for up to 10% of the ITk data) and global tracking at 100kHz.
- The system includes the possibility of an evolution to a 2 level hardware trigger with rate of up to 4 MHz.
- Subsystem was designed with all the „hooks" to allow scaling.
  - Includes a low latency (35μs) version of the hardware tracking in L1 trigger to reduce output rate to 600kHz.
- Permanent storage is at 10kHz.



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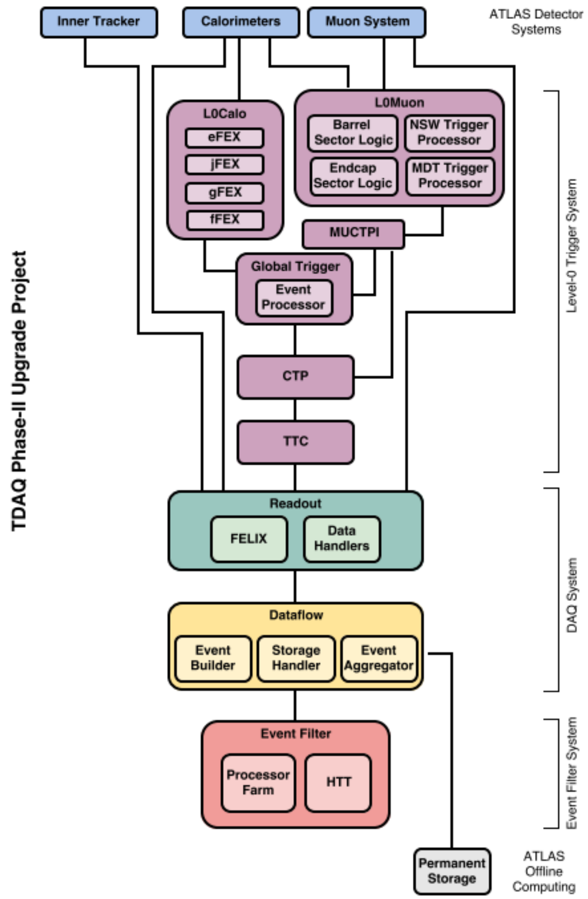
CANCELLED following reviews:

- **Architecture Review (2020)**
  Dropped the evolution idea
- **Event Filter Tracking Review (2021)**
  Dropped hardware track trigger



TDAQ in Phase-II

CERN-LHCC-2017-020

L0 Global Trigger

Goal : to bring all event data into a single processor

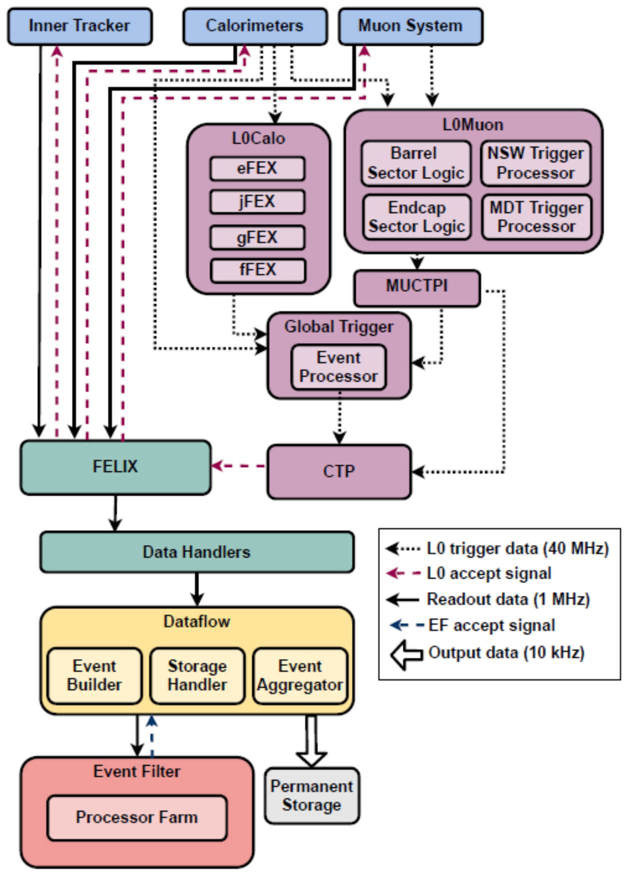
Implemented in firmware on FPGAs

Calorimeter and signature algorithms are similar to first steps of current existing HLT:

- Electrons & Photons improved with Strip information
- Taus improved with strip and topo-cluster information
- Electron, muon and Tau isolation improved with topo-cluster
- Jet & Missing Transverse-E reconstructed with topo-clusters

UK Involvement

- Hardware design, production and testing
- Firmware electron and photon algorithms
- Infrastructure hardware



TDAQ in Phase-II

CERN-LHCC-2017-020

Data Acquisition

- Goal : **F**ront **E**nd **LI**nk e**X**change routes detector data between front-end Links and COTS networks
- Storage Handlers hold event data for asynchronous access by the EF
- Data Handlers provide data aggregation, sub-detector specific processing and monitoring on commodity servers

UK Involvement:

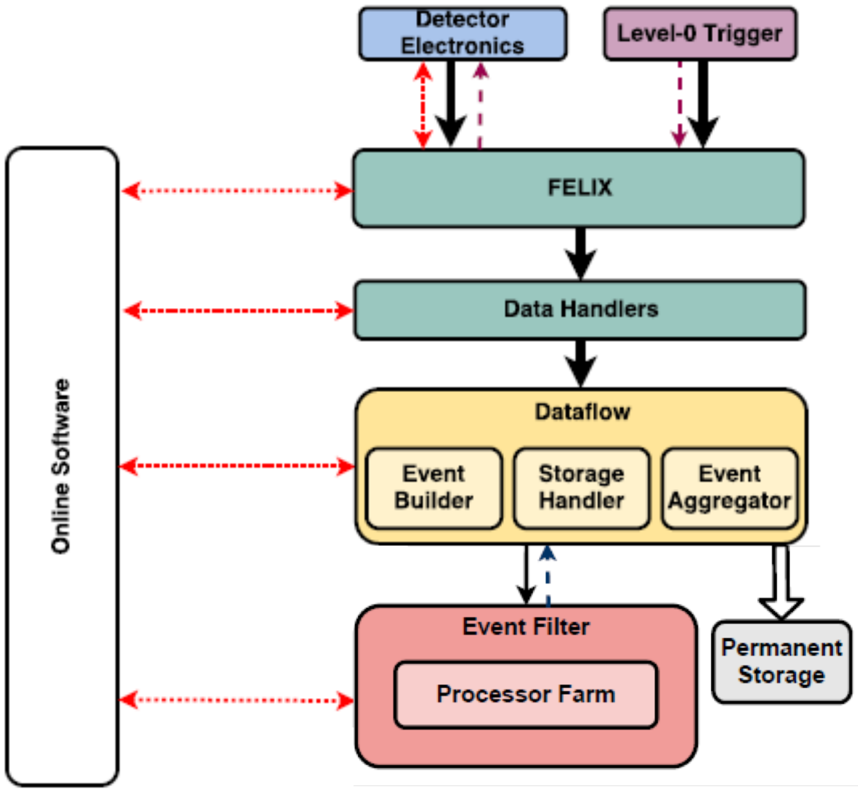
- Readout: FELIX & Data Handler software and integration
- Dataflow: Storage Handler software

Event Filter

- Goal: Provide software running on commodity processors
- AthenaMT framework: upgraded from Phase I
- Interface to dataflow and Hardware Track Trigger (HTT)
- Provide a fast initial rejection using Level-0 and regional HTT
- Reconstruction algorithms to provide pileup robust signature

UK Involvement:

- Framework, data access, ITk tracking, muon reco'n
- Evaluation of accelerator (GPU etc)
- Server hardware



Software and Simulation

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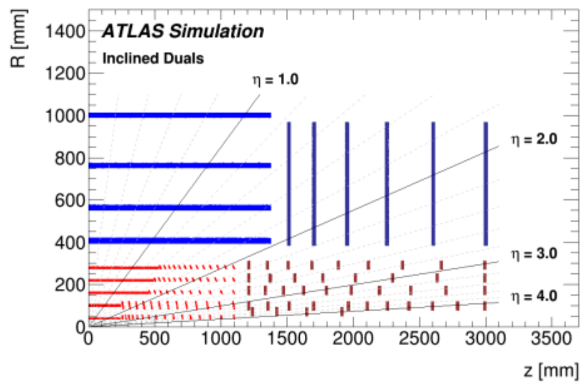
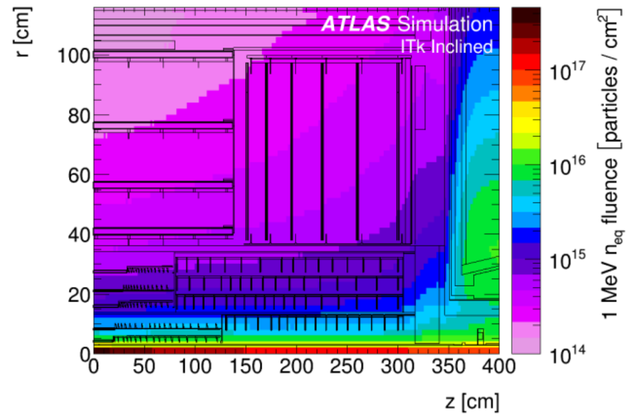
Computer architectures changing:

- Speed and efficiency to cope with the increases in data volumes and complexity
- Requires a computing model to adapt to changing hardware and computing architectures
- Multi cores, low memory/core
- Existing software approach will not scale to meet requirements
- New framework & algorithms/codes needed
- Efficient utilization of computing resources in a flat-cash world is a major challenge.



UK efforts in 4 key areas

- Frameworks
  - Gaudi Framework (scheduler), multi-threading with ATHENA-MT
- Offline tracking software and performance
  - Simulation of layouts, reco-studies, timing studies, Vtx in dense environments
  - comparisons with Run-II
- Core Simulation
  - ATHENA compliance with the Integrated Software Framework
- Radiation Environment simulation
  - radiation modeling, damage modeling



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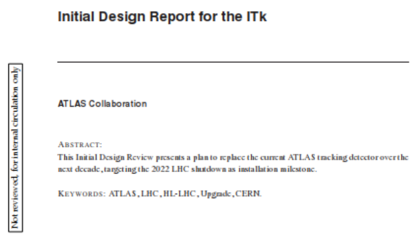
Conclusions

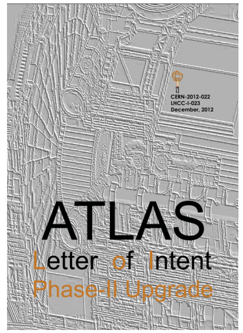
- An exciting program of frontier, and hopefully discovery, physics that takes us to 2040 and beyond.
- The UK has a significant investment in the upgrade, firmware and software and we are involved in broad range of upgrade activities.
- The UK has always provided, and continues to provide, leadership in all of the areas where we are engaged. This is at multiple levels inside the international projects. This is important.
- The construction TDRs are approved and preparation for production has started.
- Projects are now baselined and have gone into the tracking phase.
- Pre-production period has started in many tracker areas
  - most of strips
  - pixel modules and half-rings.

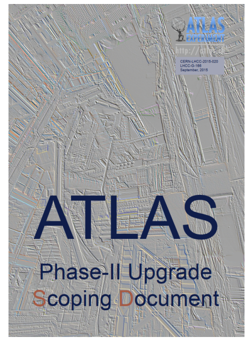
Spares

Links to some useful documents

- 2012 - Phase II Letter of Intent (148 pages)
  - https://cds.cern.ch/record/1502664/files/LHCC-I-023.pdf
- 2014 The Initial design review (146 pages):
  - https://cds.cern.ch/record/1952548?
- 2015 The scoping document: (210 pages)
  - https://cds.cern.ch/record/2055248/files/LHCC-G-166.pdf
- 2017 The Strip tracker Technical Design Report (505 pages)
  - https://cds.cern.ch/record/2257755/files/ATLAS-TDR-025.pdf
- 2018 The Pixel tracker Technical Design Report (433 pages)
  - https://cds.cern.ch/record/2285585/files/ATLAS-TDR-030.pdf
- 2018 TDAQ Technical Design Report (608 pages)
  - https://cds.cern.ch/record/2285584/files/ATLAS-TDR-029.pdf
- 2018 Muon Spectrometer Technical Design Report (408 pages)
  - https://cds.cern.ch/record/2285580/files/ATLAS-TDR-026.pdf
- 2018 Liquid Argon Calorimeter Technical Design Report (271 pages)
  - http://cdsweb.cern.ch/record/2285582/files/CERN-LHCC-2017-018.pdf
- 2018 Tile Calorimeter Technical Design Report (300 pages)
  - http://cdsweb.cern.ch/record/2285583/files/CERN-LHCC-2017-019.pdf
- 2018 Technical Proposal for High Granularity Timing Detector (154 pages)
  - http://cdsweb.cern.ch/record/2623663/files/CERN-LHCC-2018-023.pdf

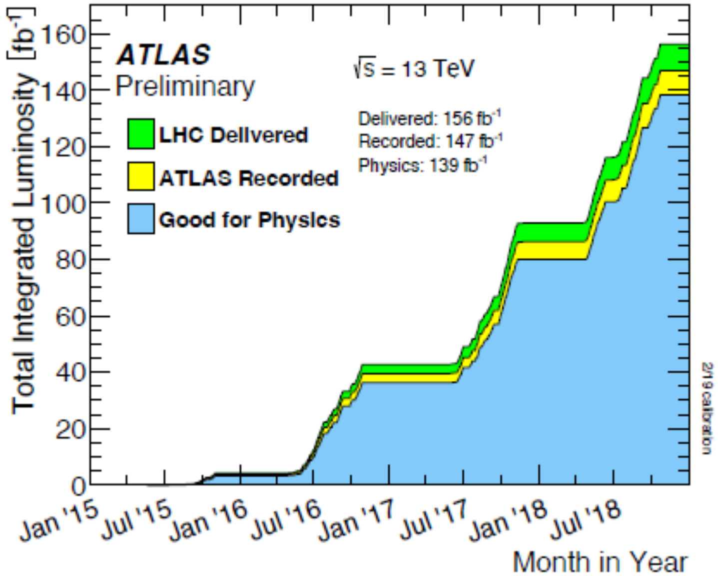






The Run-2 dataset (2015-2018)

Excellent data-taking (94.2%) and data quality (94.6%) efficiency

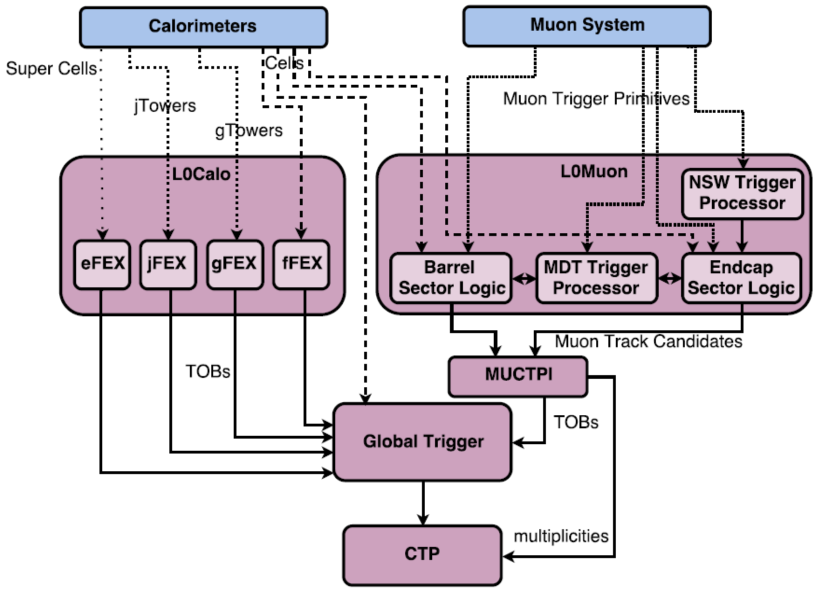


Particle	Produced in 140 fb^{-1} pp at $\sqrt{s}$ = 13 TeV	
Higgs boson	7.8 million	
Top quark	275 million	(115 million tt)
Z boson	8 billion	($\rightarrow \ell\ell$, 270 million per flavour)
W boson	26 billion	($\rightarrow \ell\nu$, 2.8 billion per flavour)
Bottom quark	~160 trillion	(significantly reduced by acceptance)

With the excellent object performance and precise calibrations, we have in our hands the richest and best understood hadron collision data sample ever recorded — a huge treasure, and yet only a small fraction of what is still to come

ATLAS Level-0 architecture

CERN-LHCC-2017-020



Level-0 upgrade:

- Added Info from Muon and Calorimeters
- **L0calo** new in Phase I and extending Feature Extraction (**FEXs**) in Phase II for fwd EM and jets
- **L0Muon** inclusion data from MDT, New Small Wheel (extend |eta|<2.6) to improve the muon trigger coverage.
- **Global Trigger** new subsystem of the Level-0 Trigger, will perform offline-like algorithms on full-granularity calorimeter data and make topo

- **Central Trigger –** new Central Trigger Processor; new Muon-to-CTP Interface

UK involvement in upgrades

- Includes:
  - Project Management (WP0)
  - L1 Calo Trigger upgrade, Phase-I (WP7)
  - L1 Calo Trigger upgrade, Phase-II (WP2)
  - ~~Hardware Track-Trigger, Phase II (WP3)~~
  - DAQ and Event Filter, Phase-II (WP4)
  - Computing & Simulation (WP5, WP10)
  - High Level Trigger, Phase-I (WP9)
  - Strip Modules (WP12)
  - Pixel Modules (WP13)
  - Strip Cores (WP14)
- and:
  - Strip Module Mounting (WP15)
  - Pixel half rings (WP16)
  - Strip Integration (WP 17)
  - DAQ Systems & Irradiation Support (WP18)
  - Pixel Module Mounting (WP19)
  - Pixel EndCap Integration (WP20)
- and
  - Contributions to common ATLAS infrastructure