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Porting Lattice QCD benchmark to upcoming STX stencil/tensor accelerator

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Developed under the European Processor Initiaive (EPI) the STX stencil/tensor accelerator aims to achieve a 5-10x higher energy efficiency over general purpose compute units.
The architectue consists of specialiced MIMD compute units which are supported and controlled by RISC-V cores.

We describe a co-design effort between hardware, software, and application development focused around porting a LQCD benchmark to this new architecture.

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