Lattice 2024



Contribution ID: 324 Type: Poster

Porting Lattice QCD benchmark to upcoming STX stencil/tensor accelerator

Tuesday, 30 July 2024 17:15 (1 hour)

Developed under the European Processor Initiaive (EPI) the STX stencil/tensor accelerator aims to achieve a 5-10x higher energy efficiency over general purpose compute units.

The architectue consists of specialized MIMD compute units which are supported and controlled by RISC-V cores.

We describe a co-design effort between hardware, software, and application development focused around porting a LQCD benchmark to this new architecture.

Primary author: SCHLEPPHORST, Simon (Forschungszentrum Jülich)

Co-author: KRIEG, Stefan (JSC, Forschungszentrum Juelich/HISKP, University of Bonn)

Presenter: SCHLEPPHORST, Simon (Forschungszentrum Jülich)

Session Classification: Poster session and reception

Track Classification: Software Development and Machines