

Evolution of readout electronics, DAQ and online technology in the next 20 years. [DRD7]

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ECFA-UK meeting on the ESPP Update



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and Innovation**

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20 years is along time in Electronics



Nokia 3510i (2003-2006)

- ▶ 9MB 'memory'
- ▶ 96x65 pixel display
- ▶ First with rudimentary internet (GPRS/WAP), up to 114kbps
- ▶ £530 inflation adjusted
- ▶ The numbers have gotten bigger, but there is more to it:
 - ▶ I don't think anyone 20y ago would imagine phones would replace desktop/laptops for most functionality.
- ▶ Are we due a similar transition in how we look at TDAQ and readout?

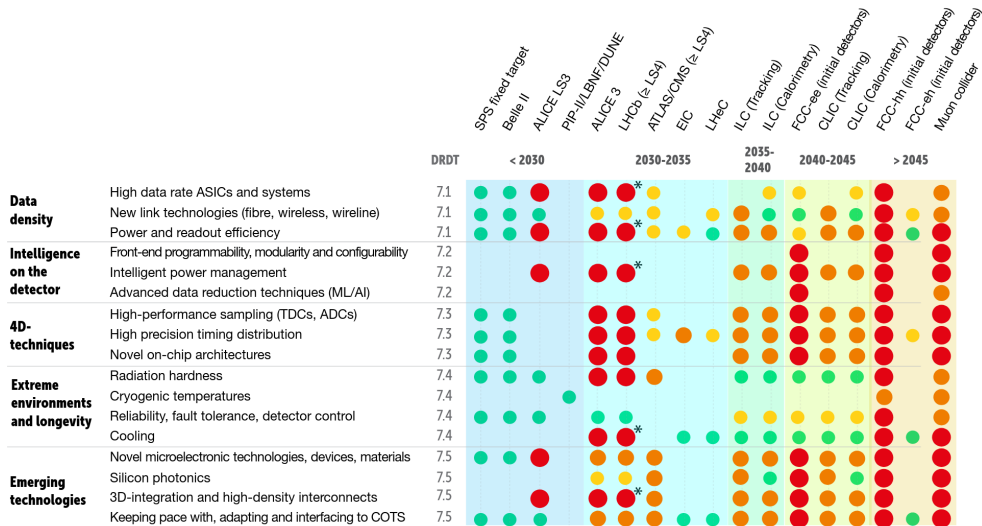


iPhone 16 (2024)

- ▶ 128GB storage
- ▶ 2556x1179 pixel display
- ▶ Used more for internet than calls/messaging, WiFi7 up to 46Gbps.
- ▶ £799 now

What is DRD7?

- ▶ The [ECFA Detector Roadmap](#) (2021) Identified R&D needs in the electronics theme as follows:



● Must happen or main physics goals cannot be met ● Important to meet several physics goals ● Desirable to enhance physics reach ● R&D needs being met

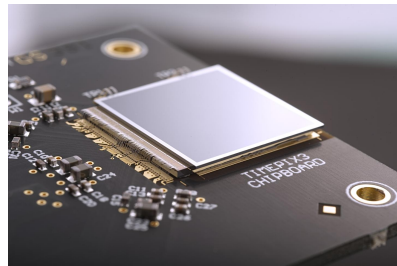
The DRD 7 proposal

- ▶ From early 2023, DRD7 has sought community input into R&D projects connected to the work packages identified in the roadmap
- ▶ This resulted in an [R&D collaboration proposal](#) released in June this year
- ▶ Individual proto-collaborations have formed, met, and started planning ahead of the MoU stage.

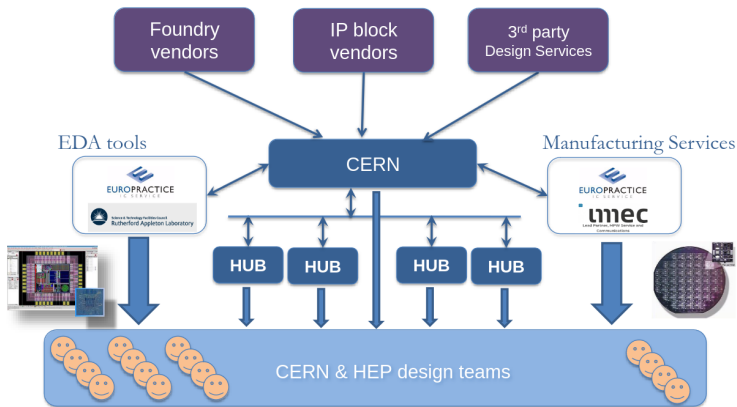
WP7.1	PROJECTS
Data density and power efficiency	7.1a Silicon Photonics transceiver development 7.1b Powering next generation detector systems 7.1c Wireless Data And Power Transmission (WADAPT)
WP7.2	
Intelligence on the detector	7.2b Radiation tolerant RISC-V SoC 7.2c Virtual electronic system prototyping
WP7.3	
4D and 5D techniques	7.3a High performance TDC and ADC blocks at ultra-low power 7.3b1 Strategies for characterizing and calibrating sources impacting time measurements 7.3b2 Timing distribution techniques
WP7.4	
Extreme environments	7.4a Device modelling and development of cryogenic CMOS PDKs and IP 7.4b Radiation resistance of advanced CMOS nodes 7.4c Cooling and cooling plates
WP7.5	
Backend systems and COTS components	7.5a DAQOverflow 7.5b From FE to BE with 100GbE
WP7.6	
Complex imaging ASICs and technologies	7.6a Common access to selected imaging technologies 7.6b Shared access to 3D integration
WG7.7	
Tools and Technologies	7.7 A Hub-based structure for ASICs developments

- ▶ The UK has historic strengths in TDAQ, Online and Electronics.
- ▶ As a result, UK involvement in at least one project in each work package
- ▶ Given the scale of involvement, I won't describe everything here today, but will highlight a few overarching themes.

- ▶ ASICs are used by every experiment
 - ▶ CMS & ATLAS have about 35 different designs
- ▶ Take time to design, manufacture and test
- ▶ Newer processes have even longer lead times and higher costs
 - ▶ Financial constraints on number of respins any one subdetector can afford, challenging to maintain expertise.
- ▶ Motivation to avoid future 'ASIC crisis' scenarios through common tools and shared expertise



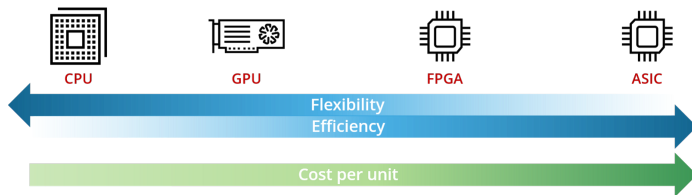
ASIC activities



- ▶ Several themes are addressing common needs through shared IP blocks
- ▶ Additional DRD 7 theme on technologies and tools to provide easier access to facilities and expertise
- ▶ UK involvement and leadership at both the theme and project level.

CPU, GPU, FPGA, and ASICs

Tradeoffs



▶ Online evolution in recent years has become increasingly COTS based

▶ Benefits:

- ▶ economy of scale
- ▶ standardisation
- ▶ usually good support and upgrade pathways

▶ Caveats:

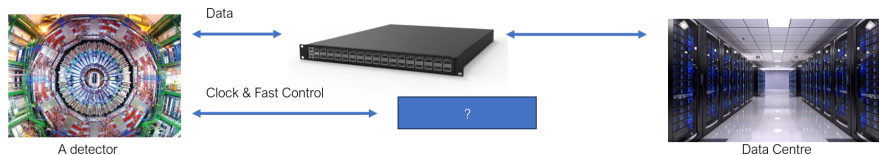
- ▶ We're (usually) not the target market
- ▶ It takes training and effort to develop for COTS
- ▶ Technology evolution is fast and hard to predict
- ▶ Choosing the right technology needs extensive R&D.

Heterogeneous benchmarking



- ▶ COTS theme aims to:
 - ▶ **Identify & Benchmark** common TDAQ algorithms/workflows on existing and new (FPGA/GPU/CPU/XPU) architectures as they become available
 - ▶ **Develop** optimised 'reference' implementations of these algorithms/workflows
 - ▶ **Maintain** a community-led repository of these implementations and their benchmarks
- ▶ Think **Stack Overflow** for TDAQ development
- ▶ Aim is to provide COTS TDAQ algorithm implementations for COTS hardware and maintain knowledge of what is cost effective as hardware evolves.
- ▶ UK leadership and significant uptake from UK institutes

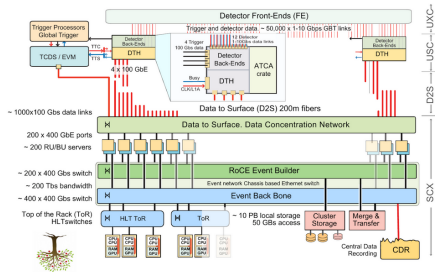
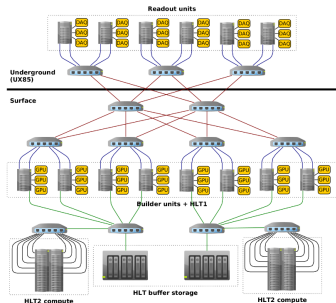
From Front- to Back-end



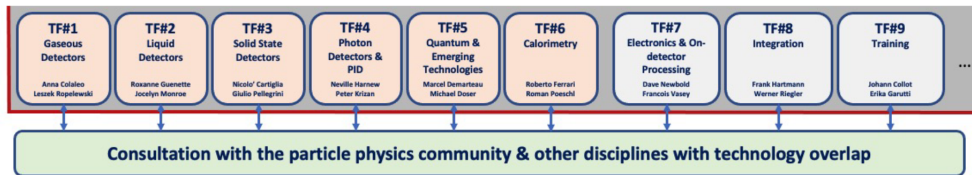
- ▶ Transition to COTS interfaces for future DAQ connectivity
 - ▶ Write 100GbE straight from the frontend
 - ▶ Use COTS or nearly-COTS network switching as a commodity DAQ.
- ▶ Two 'sub-projects':
 - ▶ using COTS switches to handle data-streams from the Front-End to Network Interface Cards (NICs) or even DAQ processors (the “No backend” approach)
 - ▶ design a COTS-based high-density switch bridging the detector environment to the COTS/DAQ world (the “Smart Switch” approach)
- ▶ These are coupled with ASIC IP development to implement 100Gb Ethernet cores for future frontends.

So what will the future look like?

- ▶ The project proposals in DRD7 loosely point to a common trend:
 - ▶ Modular designs that suit or can be made to suit a variety of future experiments
 - ▶ Standardisation favouring off-the-shelf approaches
 - ▶ Heterogeneity/interoperability of TDAQ software and tools
- ▶ This may be hedging bets, given the future is not yet certain, but there is a hint of this evolution appearing already in the HL-LHC upgrades.



Connections to other DRDs



- ▶ Paraphrasing the DRD7 coordination:
- ▶ Electronics is of importance to (nearly) all the detector R&D projects. Development of specific electronics, covering direct needs of R&D projects, is handled in respective DRDs.
 - ▶ Each DRD has a named contact to liaise with DRD7 on areas of common interest
- ▶ However, DRD7 aims to focus on low TRL developments, targeting more transformative R&D.
- ▶ Open forums within the DRD7 themes will provide an opportunity for interested parties in other DRDs to participate and contribute to discussions on important DRD7 topics.



- ▶ [3rd DRD 7 workshop](#) held 9th-10th September at CERN
- ▶ The proto-projects are loosely planned out to 2026, with milestones to be refined based on personpower commitments and available funding ahead the MoU drafting process
- ▶ UK involvement is currently best-effort as no dedicated funding mechanism (yet).
- ▶ Ten UK institutes are signed on to the first DRD7 proposal round (Imperial, QMUL, RAL, UCL, Birmingham, Bristol, RHUL, Manchester, Oxford, Warwick)
- ▶ Additional project proposals will be called for yearly, and existing proposals can be extended as the programme evolves.

Conclusions

- ▶ It's hard to predict what advances in electronics will bring over the next 20 years, but there are hints:
 - ▶ ASICs in particular need long development times, so we can't afford to wait
 - ▶ Adapting to commercial, off-the-shelf technologies looks appealing
- ▶ The DRD7 proposal has strong representation and leadership from the UK. This should be noted in our EPPSU input.

Interested in participating? Contact CF (Manchester), Marcus French (RAL), Karolos Potamianos (Warwick), Mark Prydderch (RAL), Andrew Rose (Imperial) at drd7-uk-leads@cern.ch