Silicon Vertex and Tracking sensor technologies: from LHC to FCC [DRD3]

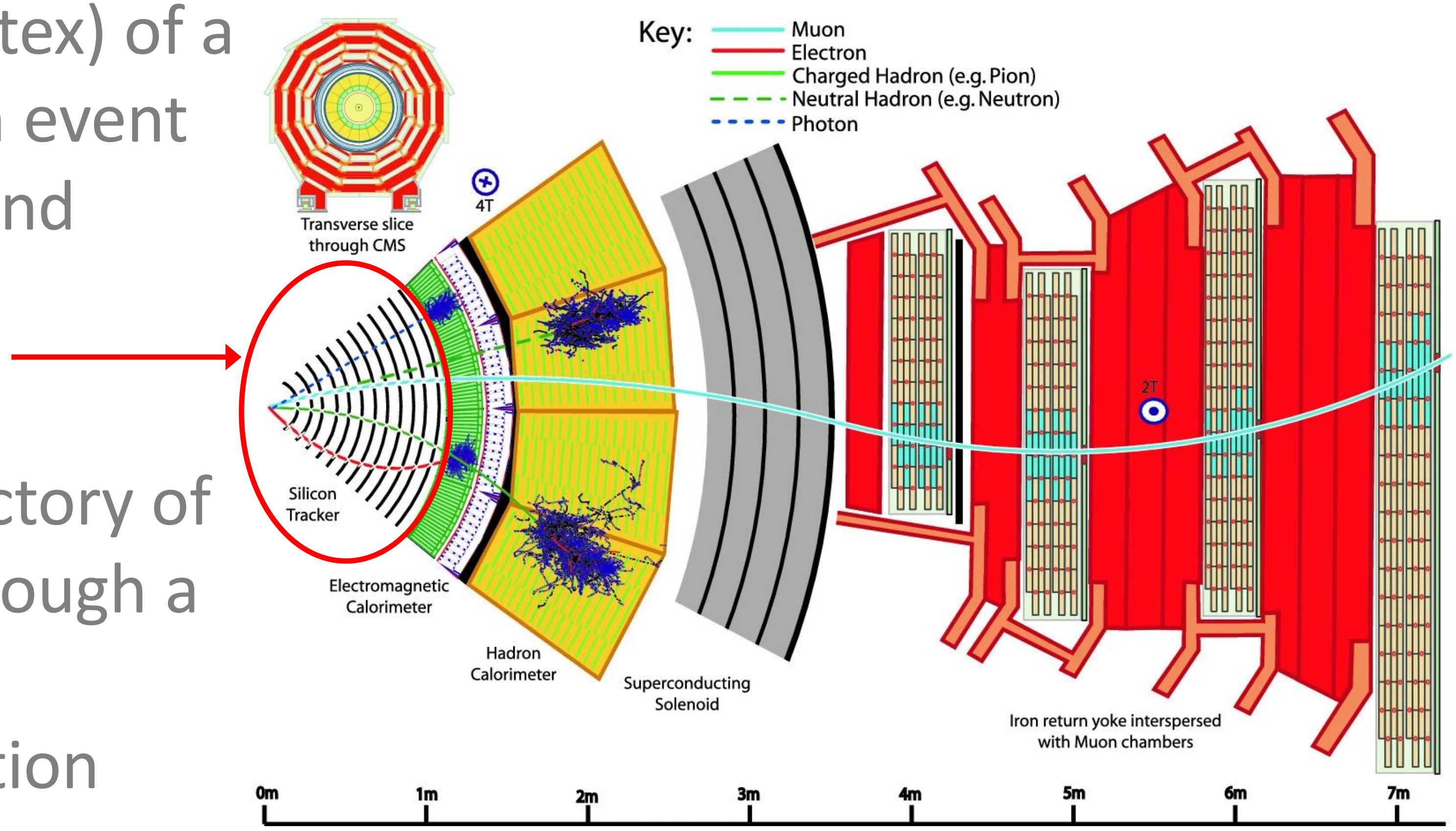
Eva Vilella
[with inputs from many others… thanks!]
University of Liverpool
vilella@hep.ph.liv.ac.uk

Overview

- Introduction: Silicon vertex and tracking detector technologies
- Current R&D for 2030s detectors
- Replacement options for ATLAS and CMS layers
- Smaller-scale detector systems for the 2030s
- Future collider requirements (FCC-ee and other e+e- colliders)
- Speculative remarks on FCC-hh
- Monolithic CMOS sensors in future detectors
- Low-mass service systems for silicon sensors
- Non-silicon sensors
- Conclusion and outlook

Silicon vertex and tracking detector technologies

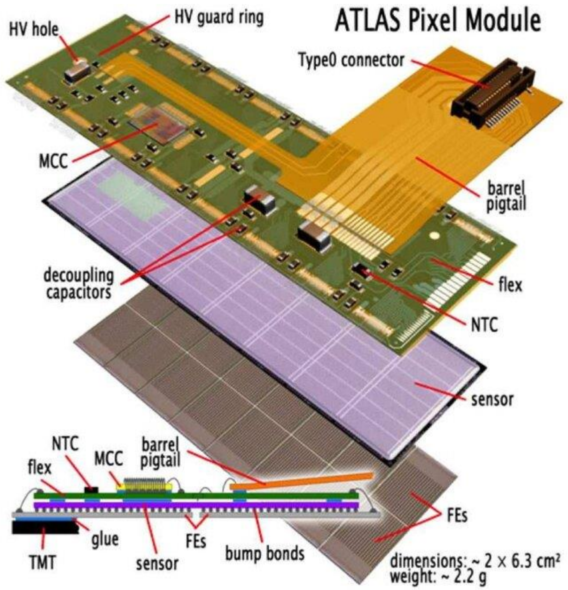
- **Particle vertexing**
  - Exact point of origin (vertex) of a particle within a collision event
  - For identifying primary and secondary vertices
- **Particle tracking**
  - Reconstructing the trajectory of a particle as it travels through a detector
  - Provides crucial information about the particle's momentum, direction and charge

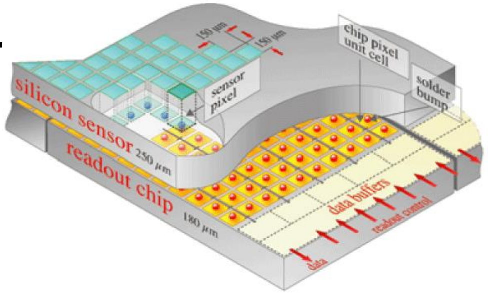


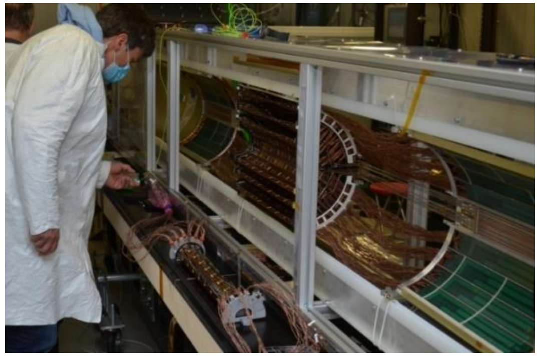
Currently at the LHC – Silicon is everywhere!

	Pixels	Strips
Hybrid	• ATLAS Pixel Detector + B-Layer • CMS Pixel Detector • LHCb VELO	• ATLAS SemiConductor Tracker • CMS Tracker • LHCb Upstream Tracker
Monolithic	• ALICE ITS 2	

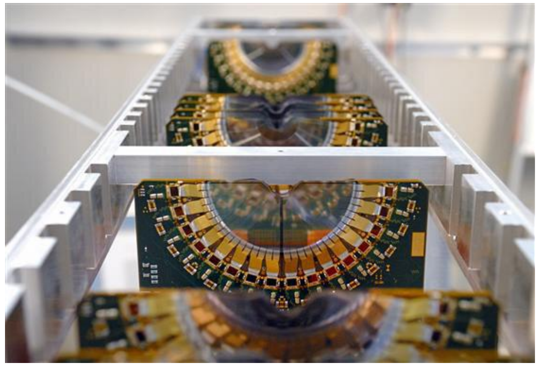
ATLAS Pixel Detector







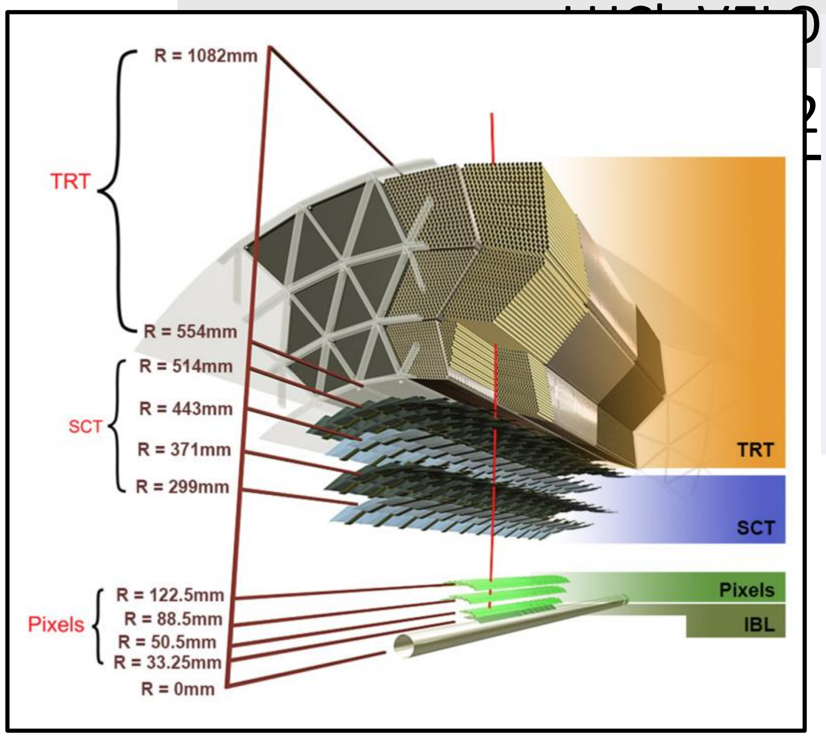
CMS Pixel Detector

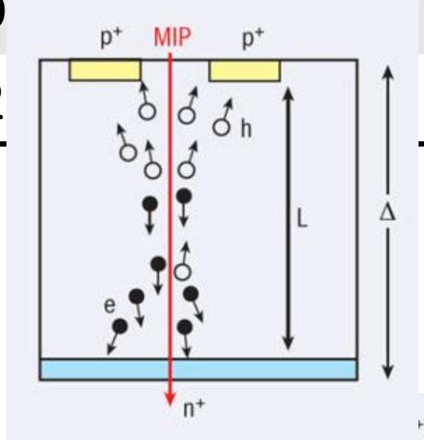


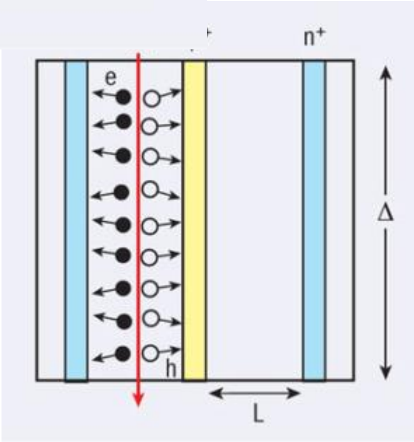
LHCb VELO

Currently at the LHC

	Pixels
Hybrid	• **ATLAS Pixel Detector + B-Layer** • CMS Pixel Detector







ATLAS Pixel Detector

Process n-on-n planar
Pixel size 50 µm x 400 µm
Thickness 250 µm
TID 50 Mrad
NIEL 1e15 n_{eq}/cm^2
Readout chip FE-I3 (0.25 µm CMOS)
Total area ~2 m^2

ATLAS Insertable B-Layer (in LS1)

Process n-on-n planar & 3D (n+, double-sided)
Pixel size 50 µm x 250 µm
Thickness 200 µm
TID 250 Mrad
NIEL 5e15 (or 1
Readout chip FE
Total area

Hybrid planar and 3D pixels with CMOS readout chip

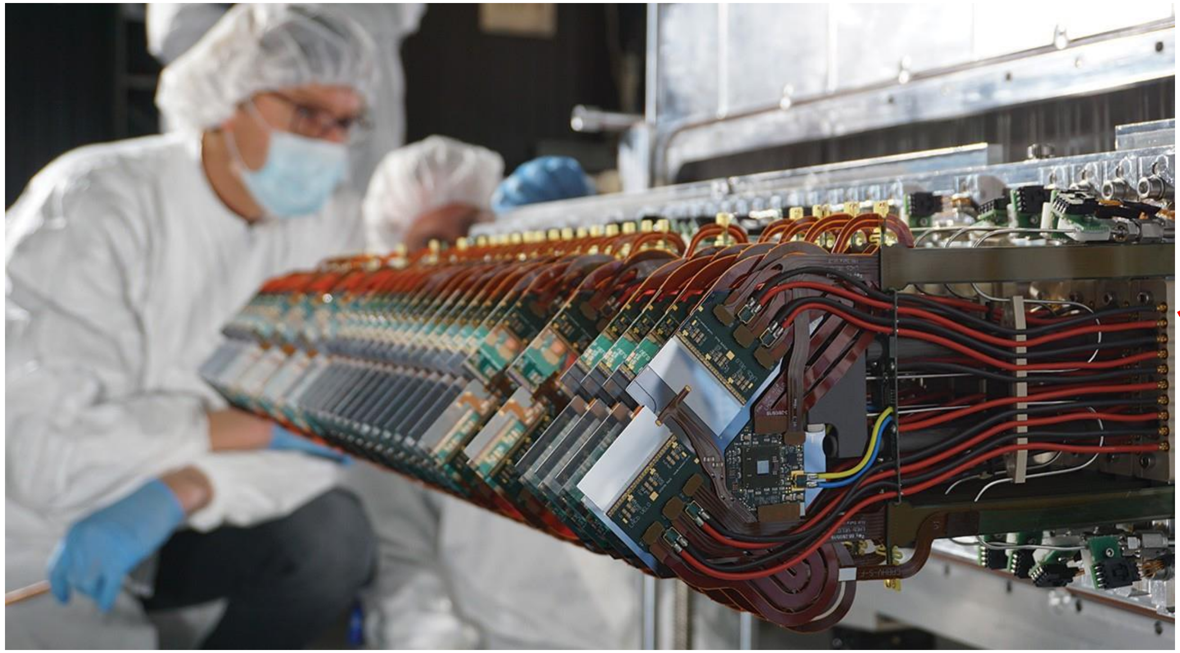
Currently at the LHC

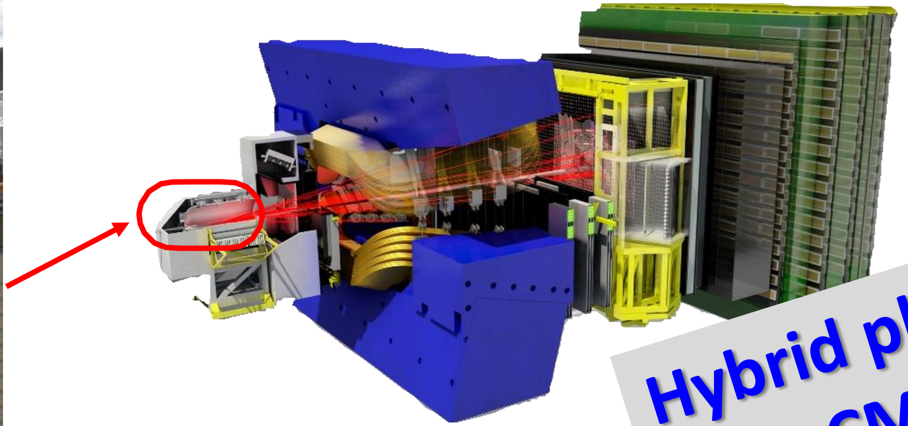
[Hybrid silicon strips before that]

	Pixels
Hybrid	• ATLAS Pixel Detector + B-Layer • CMS Pixel Detector • **LHCb VELO**
Monolithic	• ALICE ITS 2

LHCb VELO pixels (in LS2)

Process n-on-p planar
Pixel size 55 µm x 55 µm
Thickness 200 µm
TID 400 Mrad (VeloPix)
NIEL 8e15 n_{eq}/cm^2
Readout chip VeloPix (130 nm CMOS)
Total area 0.12 m^2





Hybrid planar pixels with CMOS readout chip

Currently at the LHC

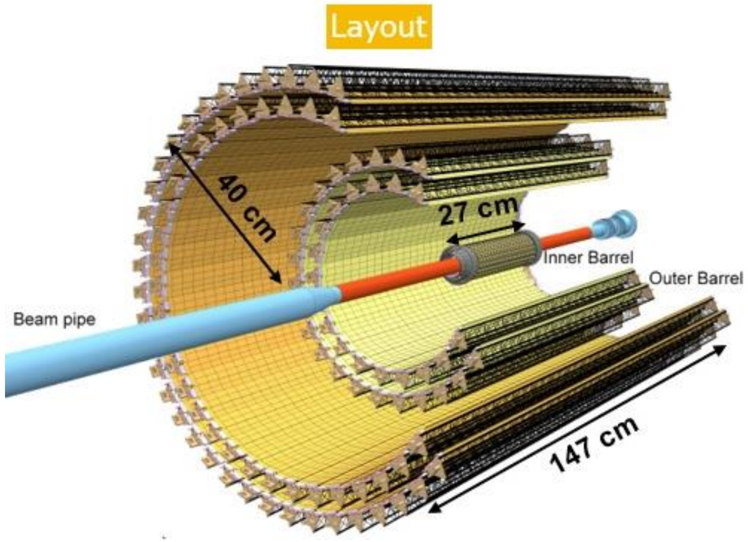
	Pixels
Hybrid	• ATLAS Pixel Detector + B-Layer • CMS Pixel Detector • LHCb VELO
Monolithic	• **ALICE ITS 2**

ALICE Inner Tracking System (in LS2)

Process Monolithic CMOS (180 nm TowerJazz)
Pixel chip Alpide (ALice PIxel DEtector)
Pixel size 30 µm x 30 µm
Thickness 50-100 µm
TID 700 krad
NIEL 1e13 n_{eq}/cm^2
Power consumption 50 mW/cm^2
Chip size 15 mm x 30 mm
Total area 10 m^2

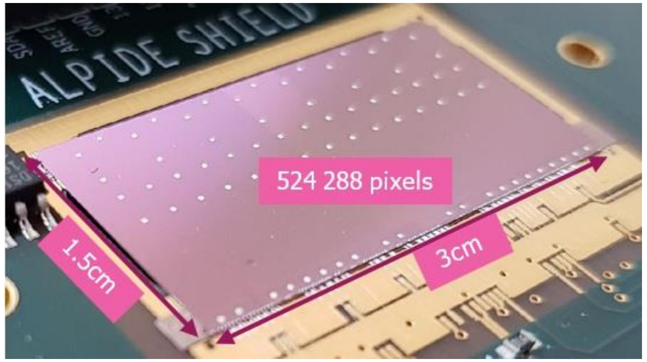
Monolithic CMOS

[Hybrid silicon pixels and strips before that]

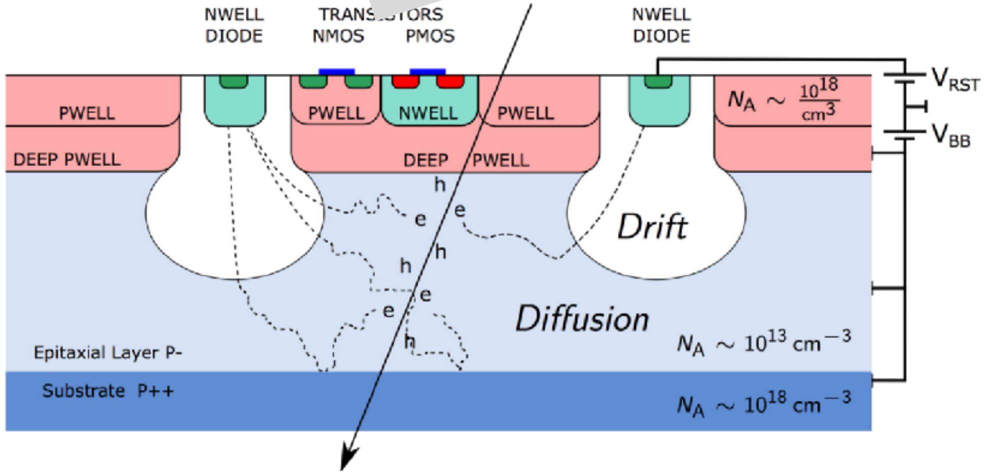


ALICE ITS upgrade ITS 2

M. Mager, NIM-A: 824 434-438, 2016



ALPIDE

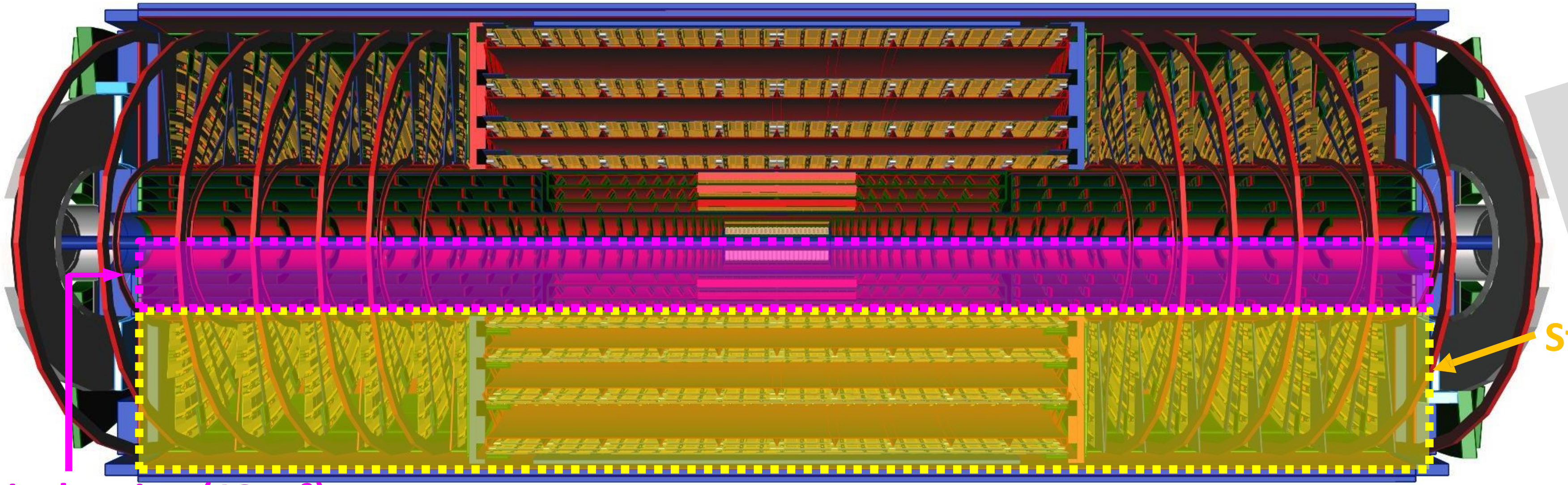


Transition to High Luminosity LHC

	Pixels
Hybrid	• **ATLAS ITk – Pixels** • CMS Pixel Detector • LHCb VELO
Monolithic	• ALICE ITS 2

ATLAS ITk Pixels

Process n-on-p planar & 3D (innermost layer)
Pixel size 50 µm x 50 µm (planar, 3D), 25 µm x 100 µm (3D)
Thickness 100-150 µm (planar), 150 µm (3D)
TID 500 Mrad (ITkPixV1)
NIEL 1e16 n_{eq}/cm^2 (ITkPixV1)
Readout chip ITkPixV1 (65 nm CMOS)
Total area 13 m^2 (pixels), 165 m^2 (strips)



Pixel region (13 m^2)

Stri region (165 m^2)

Hybrid planar and 3D pixels with CMOS readout chip

New challenges

- **Complete HL-LHC**
- **FCC-ee**
  - High precision
  - Low mass
  - Low power
- **FCC-hh**
  - Low power
  - High radiation tolerance (8e17)

DRD3

DRD3 Research topics	
WG1	Monolithic silicon sensors
WG2	Hybrid silicon technologies
WG3	Extreme fluence
WG4	Simulation
WG5	Characterisation techniques
WG6	Wide bandgap and innovative sensors materials (diamond, SiC, GaN)
WG7	Interconnections and device fabrication

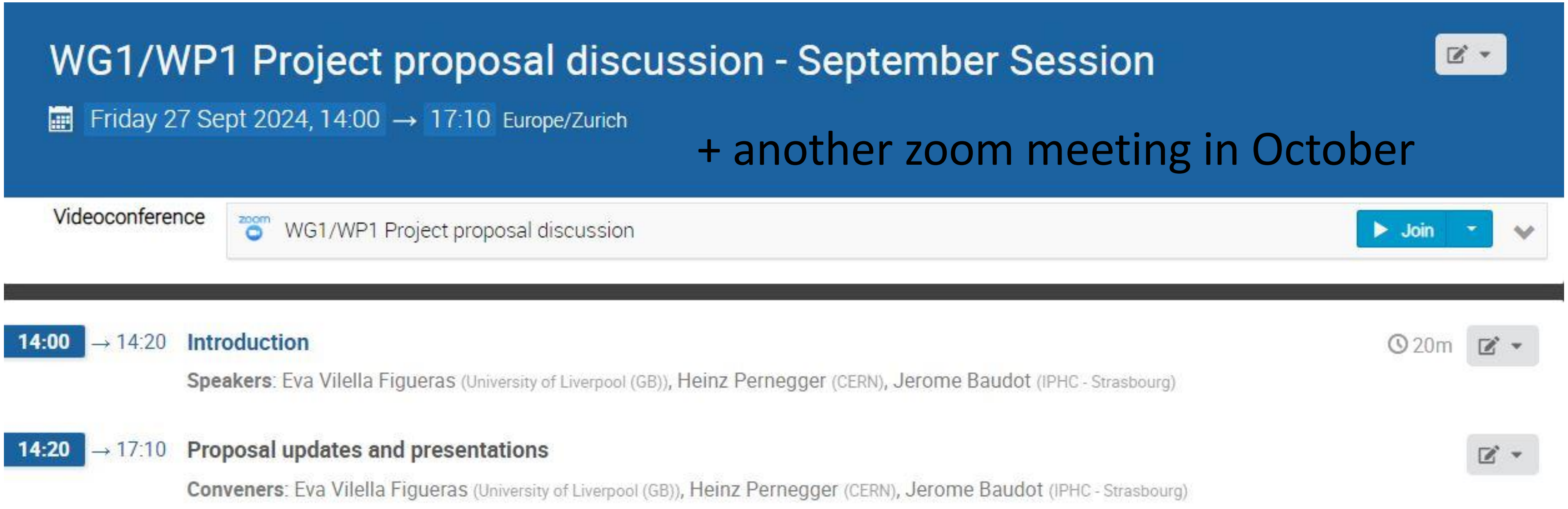
- **Pile-up mitigation by ultra-fast timing in O(10-100 ps)**
- **Sensors with fully integrated electronics, mechanics and services**
- **Large area sensors at low cost**

DRD3.1 Monolithic silicon sensors

- **Aim is to advance the performance of monolithic CMOS, combining sensing and readout elements, tackling the challenges of:**
  - Very high spatial resolution
  - Good timing performance
  - High data rate
  - High radiation tolerance
  - Keeping an affordable cost
  - Low mass
  - Covering large areas
  - Reducing power
  - And ultimately combining all these in one single device

DRD3.1 research goals <2027	
1.1	Position resolution: ≤3 µm
1.2	Timing resolution: towards 20 ps
1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
1.4	Radiation tolerance: towards e16 n_{eq}/cm^2 NIEL and 500 Mrad TID
1.5	Low-cost large-area CMOS sensors

DRD3.1 project proposals



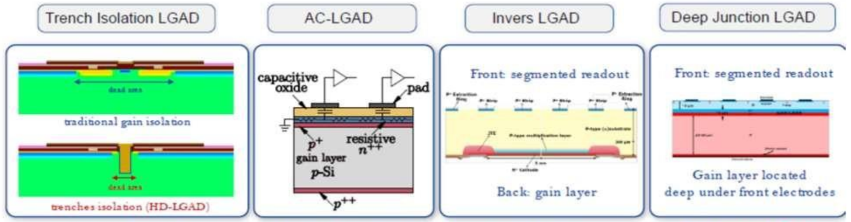
+ another zoom meeting in October

- Monolithic CMOS sensors for fast-timing (without and with gain layer for internal amplification), in several processes
- Arcadia type sensors
- Versatile CMOS sensor for several future tracking applications
- Thin radiation tolerant HV-CMOS sensors
- Radiation hard readout architectures
- Fine-pitch CMOS sensors for lepton colliders
- Ultra-low mass tracking detectors
- CMOS strips
- New processes

DRD3.2 Hybrid silicon technologies

- **Aim is to advance the performance of different sensor technologies (TI-, AC-, invers- DJ-LGAD, 3D, etc.) for several specific applications:**
  - Future upgrades beyond LHC Phase-II might use 4D layers at moderate radiation levels (1-3e15 n_{eq}/cm^2) with 10-30 µm spatial resolution
  - LHCb and FCC-hh will require >1e16 n_{eq}/cm^2
  - Radiation tolerance limited by loss of gain → material engineering or 3D possible solution at extreme fluences

DRD3.2 research goals <2027	
2.1	Reduction of pixel cell size for 3D sensors
2.2	3D sensors for timing (50 × 50 µm, < 50 ps)
2.3	LGAD for 4D tracking <10 µm, <30 ps, wafer 6” and 8”
2.4	RSD for ToF (Large area, <30 µm, <30 ps)



DRD3.6 Wide bandgap and innovative sensor materials

- WBG semiconductors can be used for **timing applications** due to the high carrier saturation velocity, and their **radiation tolerance** makes them suitable for extreme fluence with the added advantage that they can be operated without cooling.

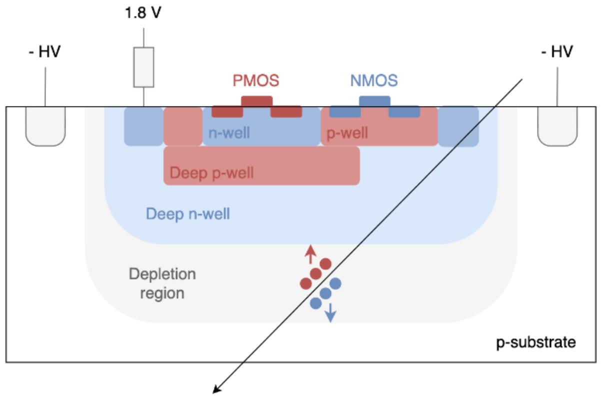
DRD3.6 research goals <2027	
6.1	3D diamond detectors
6.2	Fabrication of large-area SiC and GaN detectors, improve material quality and reduce defect levels
6.3	Improve tracking capabilities of WBG materials
6.4	Apply graphene and/or other 2D materials in radiation detectors, understand signal formation

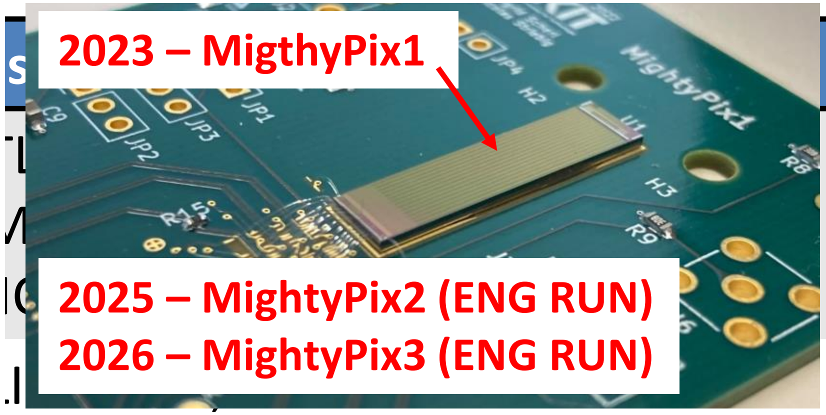
Transition to High Luminosity LHC

	Pixels	Strips
Hybrid	• ATLAS ITk – Pixels • CMS Pixel Detector • LHCb VELO	• ATLAS ITk – Strips • CMS Tracker
Monolithic	• ALICE ITS 3, ALICE 3 • LHCb Mighty Tracker & UP	

[A selection]

Transition to High Luminosity LHC

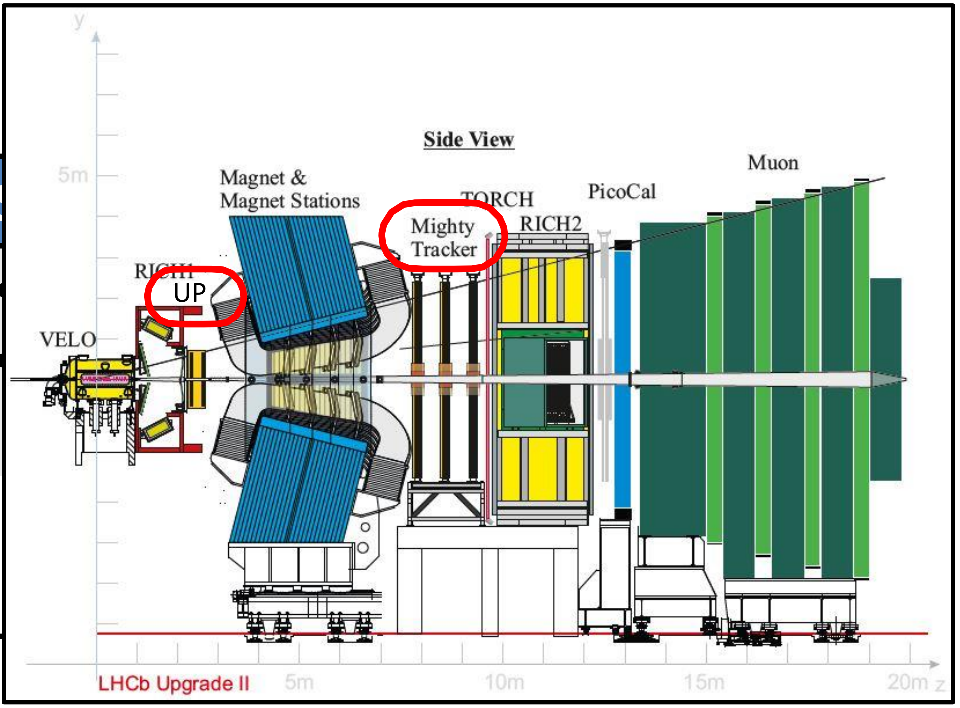




2023 – MigthyPix1

2025 – MightyPix2 (ENG RUN)
2026 – MightyPix3 (ENG RUN)

- **LHCb Mighty Tracker & UP**



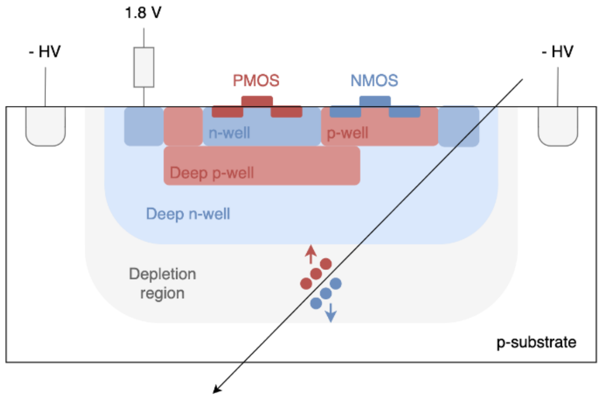
LHCb Mighty Tracker
Process Monolithic CMOS (180 nm AMS, 150 nm LFoundry HV)
Pixel size 50 µm x 150 µm
Thickness 200 µm
TID 40 Mrad
NIEL 3e14 n_{eq}/cm^2
Total area ~12 m^2 (scenario not fixed yet)

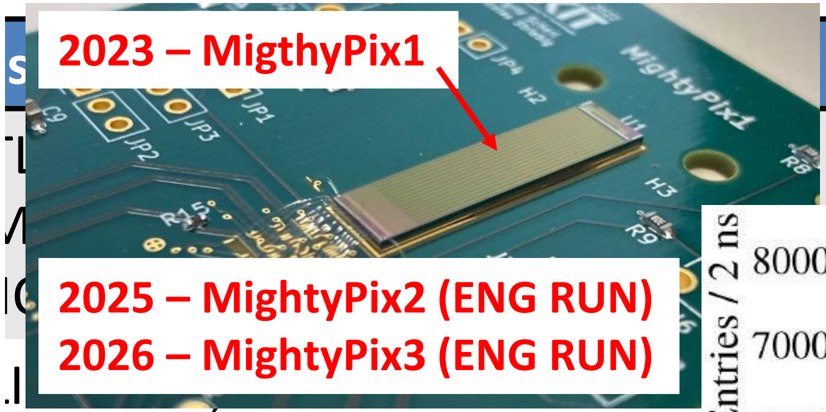
LHCb UP
Process M… ic CMOS (considering a few
… µm
… ss 200 µm
TID 240 Mrad
NIEL 3e15 n_{eq}/cm^2
Total area

Specs currently under revision

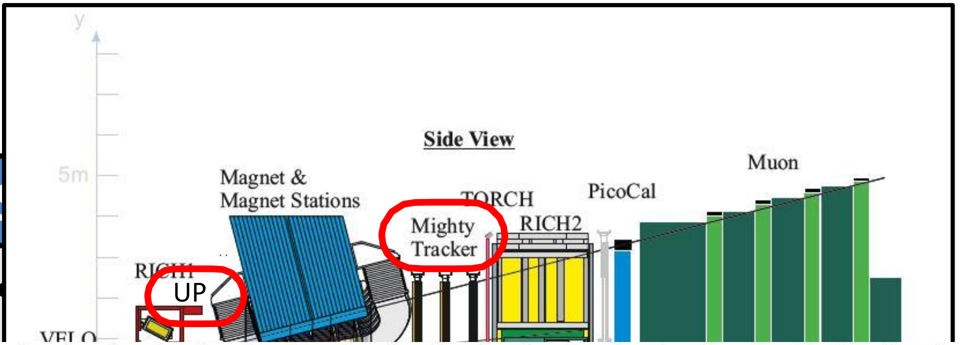
Monolithic CMOS

Transition to High Luminosity LHC



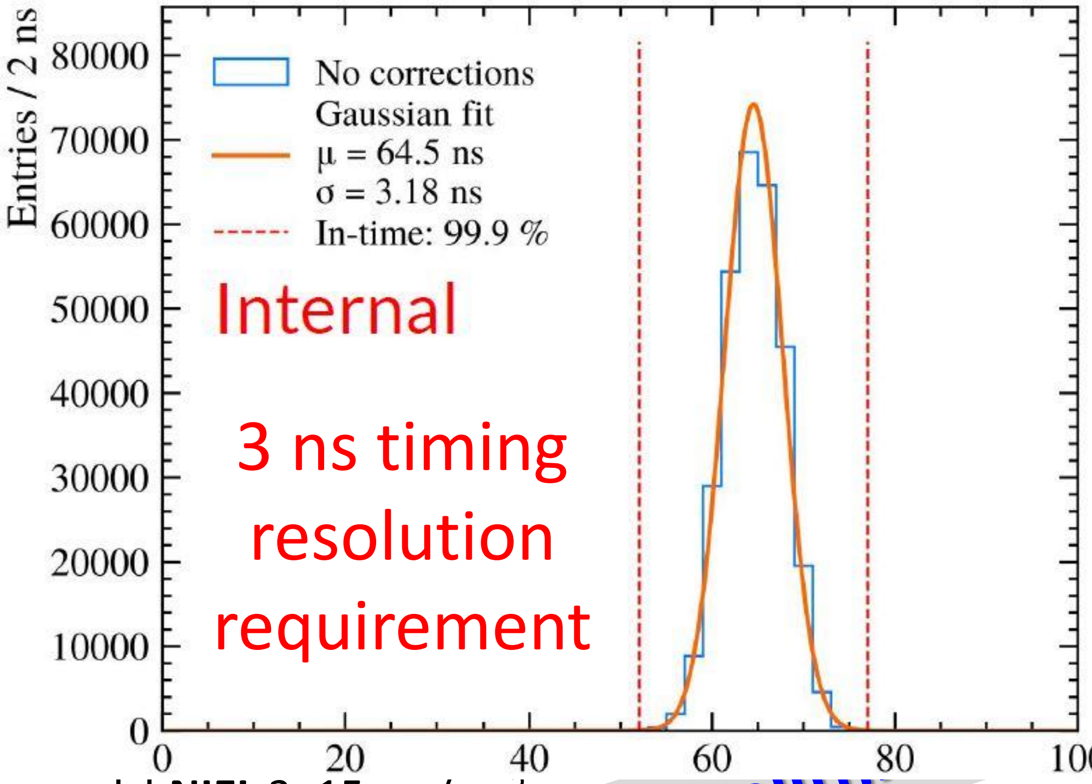


- **LHCb Mighty Tracker & UP**



LHCb Mighty Tracker
Process Monolithic CMOS (180 nm AMS, 1… nm LFoundry HV)
Pixel size 50 µm x 150 µm
Thickness 200 µm
TID 40 Mrad
NIEL 3e14 n_{eq}/cm^2
Total area ~12 m^2 (scenario not fixed yet)

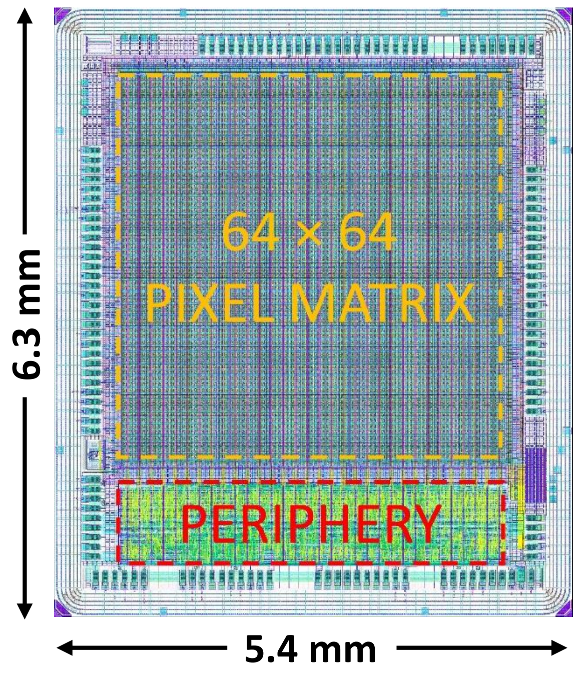
NIEL 3e15 n_{eq}/cm^2
Total area

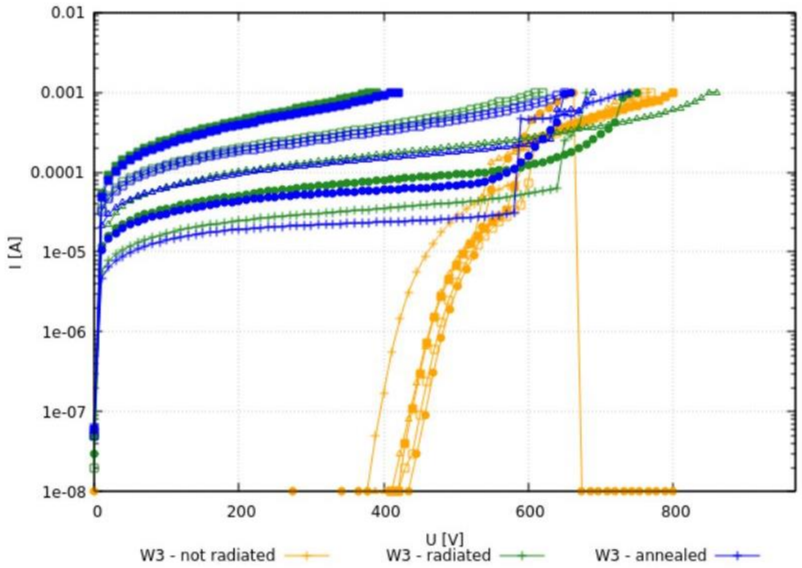


Monolit…

RD50-MPW4

- **High breakdown voltage and high radiation tolerance**
  - Multiple ring structure around the chip edge
  - Substrate backside-biasing to high voltage
- **Fabrication details**
  - 150 nm High Voltage CMOS LFoundry (LF15A)
  - P-type substrate with nominal 3 kΩ·cm high resistivity
  - 280 µm thin
- **Chip contents**
  - Pixel matrix with FE-I3 style readout
    - 64 x 64 pixels
    - 62 µm x 62 µm pixels with large collection electrode
  - Digital periphery (I2C slow control, data transmission)
- **Irradiation campaign**
  - Neutrons → several fluence from 1e14 to 3e16 n_{eq}/cm^2

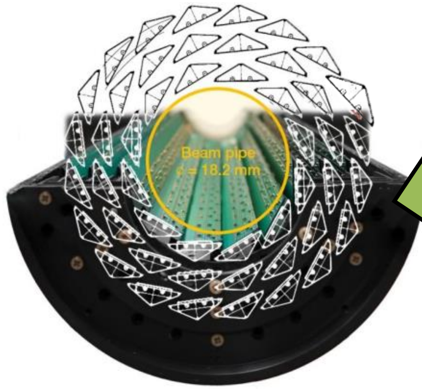




Transition to High Luminosity LHC

	Pixels
Hybrid	• ATLAS ITk – Pixels • CMS Pixel Detector • LHCb VELO
Monolithic	• **ALICE ITS 3**, ALICE 3 • LHCb Mighty Tracker & UP

ALICE Inner Tracking System 3
Process 65 nm CMOS (TPSCo) **Pixel size** **Thickness** 50 µm **TID** 10 kGy **NIEL** e13 n_{eq}/cm^2 **Power consumption** 20 mW/cm^2 **Chip size** 27 cm x 9 cm (chip stitching) **Total area** 60 m^2



ITS2

Inner Barrel

ITS3

ITS3 LoI: CERN-LHCC-2019-018

Replacing the 3 innermost layers with new ultra-light, truly cylindrical layers

- Reduced material budget by re... water cooling, circuit ... mechanical ...
- Closer to th...

Improved ver... reduc...

CMOS with low-mass low-power with large-area coverage

Transition to High Luminosity LHC

ALICE ITS3 chip development roadmap

2021

2022

2023

2024

MLR1 (Multi-Layer Reticle 1): first MAPS in TPSCo 65 nm

- Successfully qualified the 65 nm process for ITS3 (and much beyond)

ER1 (Engineering run 1): first stitched MAPS

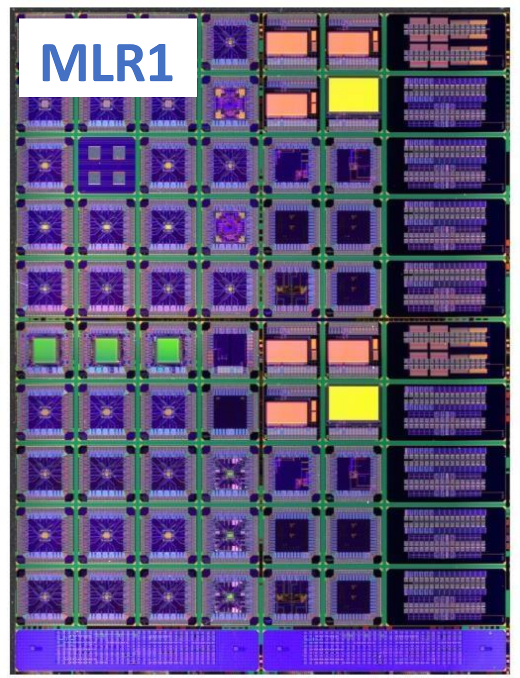
- Large design “exercise”, stitching was new
- Test campaign

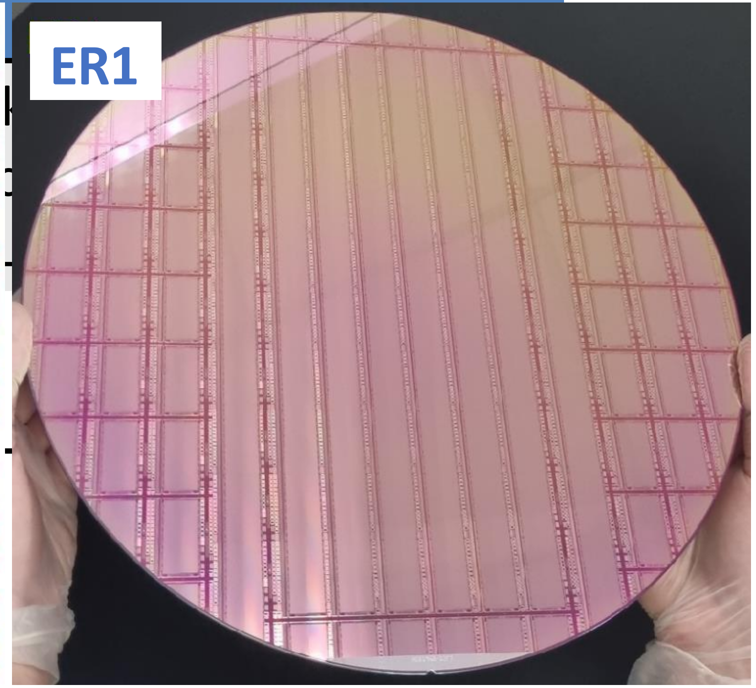
ER2 (Engineering run 2): first ITS3 prototype

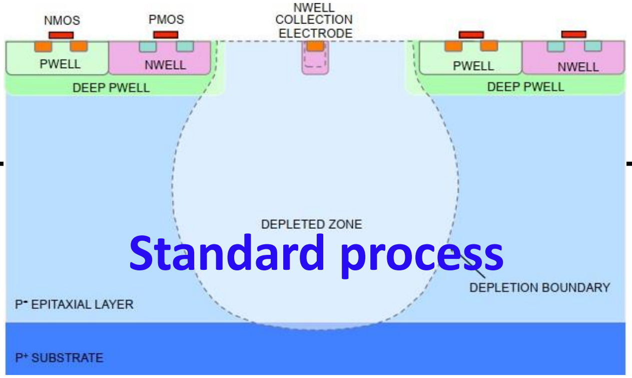
- Further ITS3 ER planned (2025?)

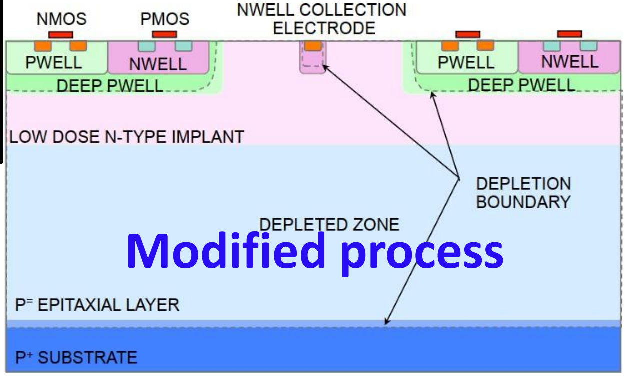
2025 -28

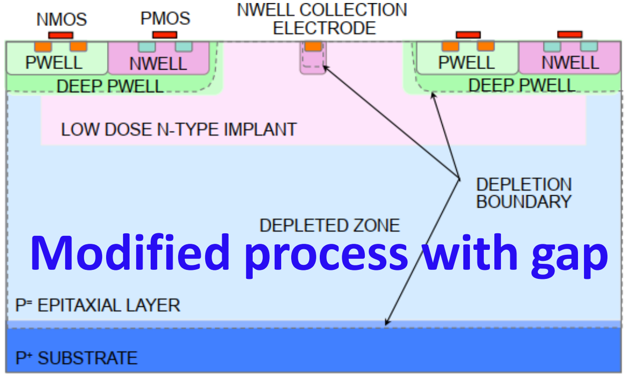
Multi-Project Reticles (MPR2, 3 and 4) (to be shared with the community)







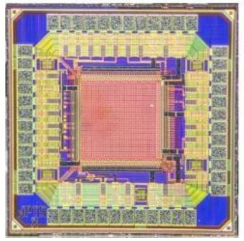




Transition to High Luminosity LHC

Prototypes (65 nm CMOS)

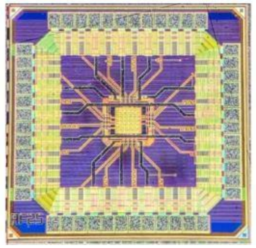
Digital Pixel Test Structure (DPTS)
- 32 x 32 pixel matrix
- Asynchronous digital readout with Time- over-Threshold information
- Pitch: 15 µm
- Only ‘modified with gap’ process

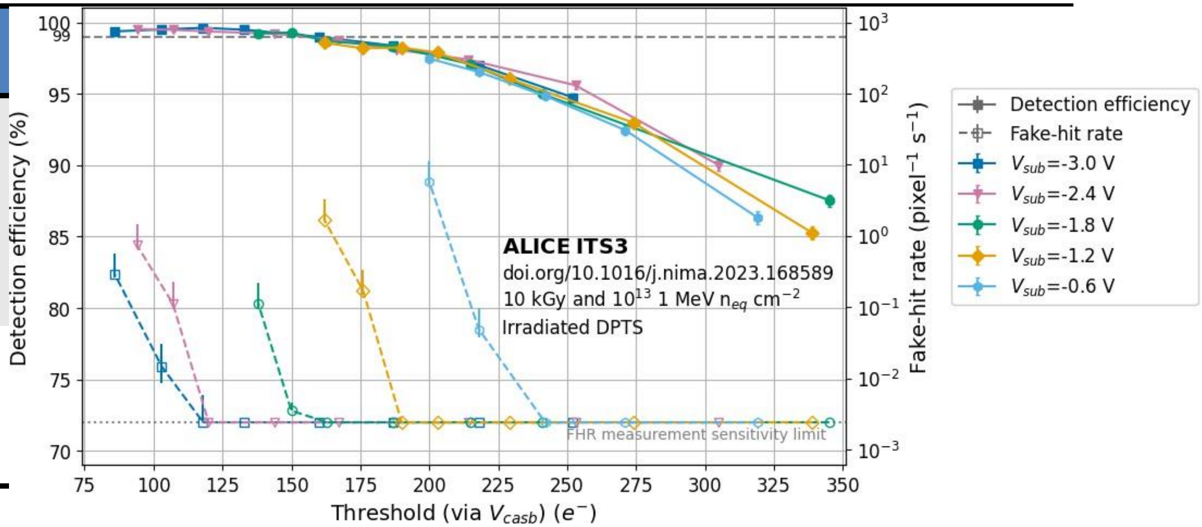


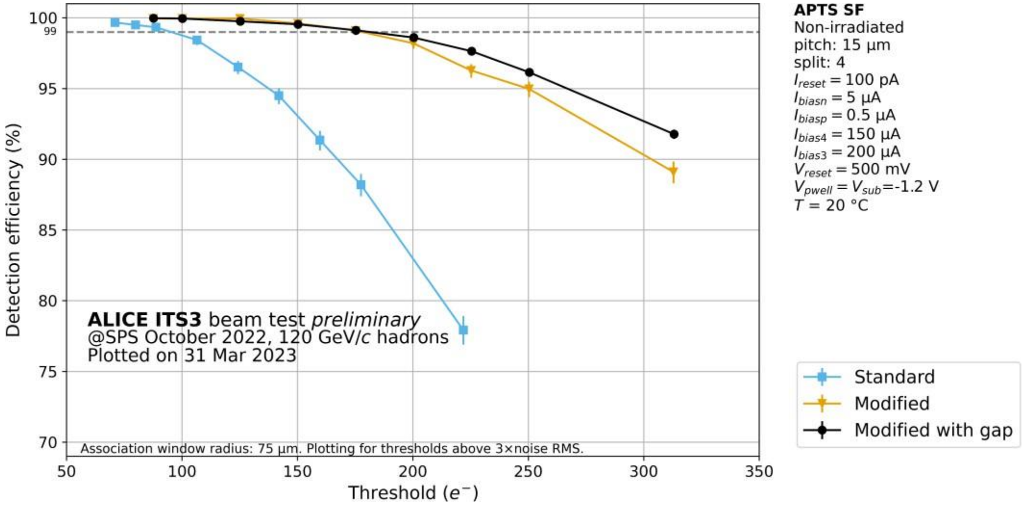
• LHCb Mighty Tracker & UP

Prototypes (65 nm CMOS)

Analogue Pixel Test Structure (APTS)
- 6 x 6 pixel matrix
- Direct analogue readout of central 4 x 4 pixels
- Two types of output drivers:
  - Source follower (APTS-SF)
  - Fast OpAmp (APTS-OA)
- Pitch: 10, 15, 20 and 25 µm







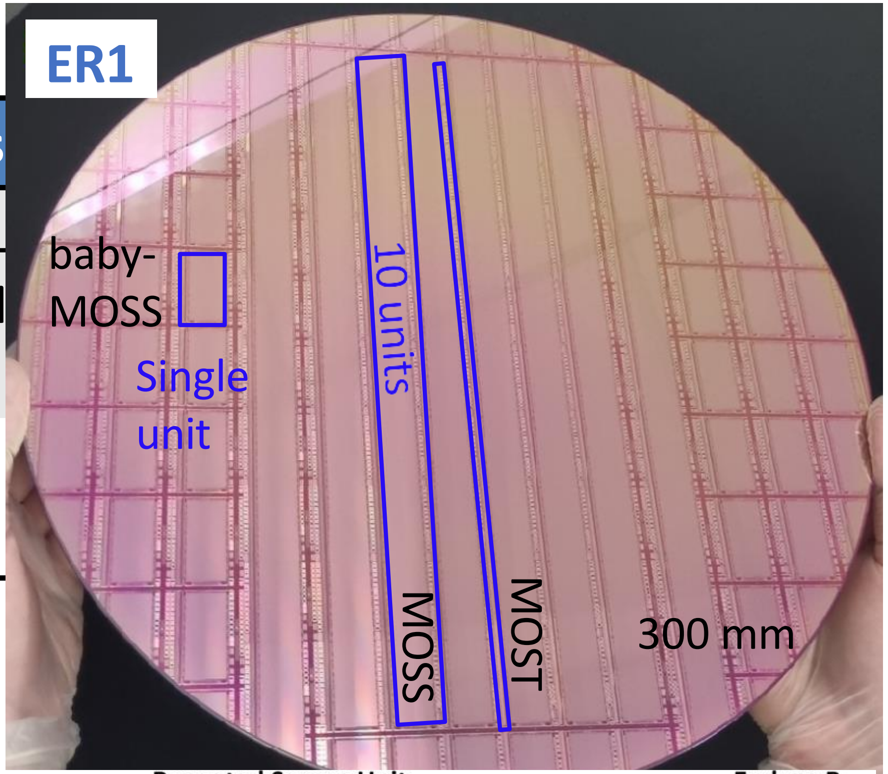
Transition to High Luminosity LHC

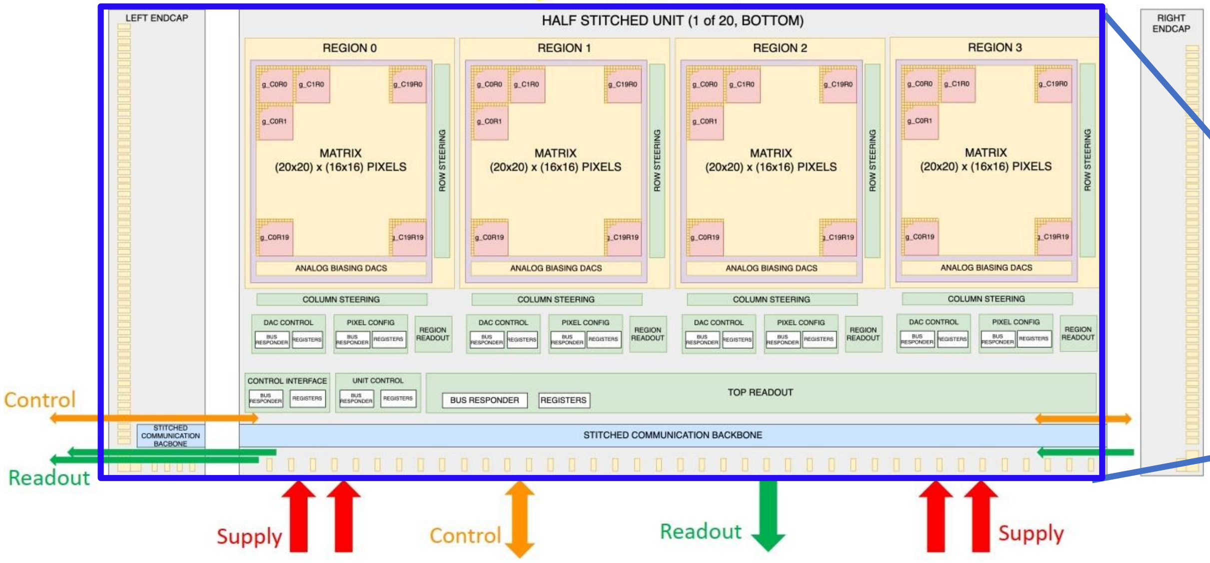
Prototype also with LFoundry 150 nm (for large area detectors)

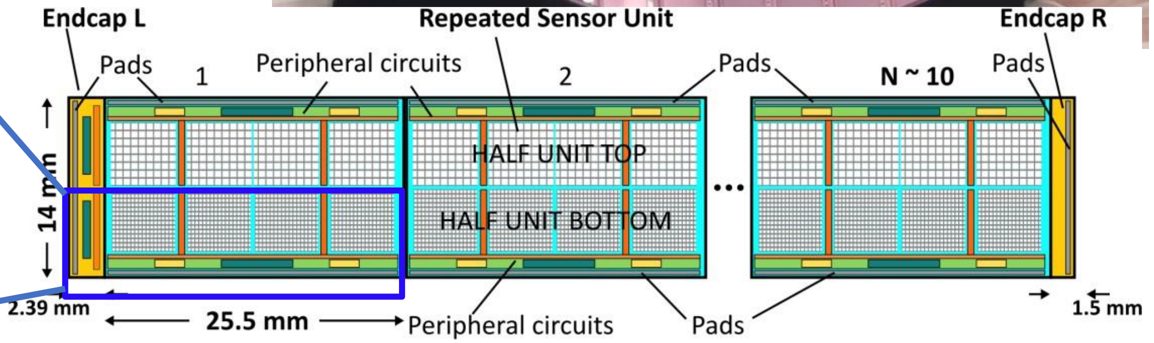
Prototypes (65 nm CMOS)

Monolithic CMOS using stitching (TPSCo 65 nm)
Flavours:

- 'MOSS'
  - 14 mm x 259 mm (6.72 Mpixels)
  - 22.5 µm x 22.5 µm and 18 µm x 18 µm
- 'MOST'
  - 2.5 mm x 259 mm (0.9 Mpixels)
  - 18 µm x 18 µm



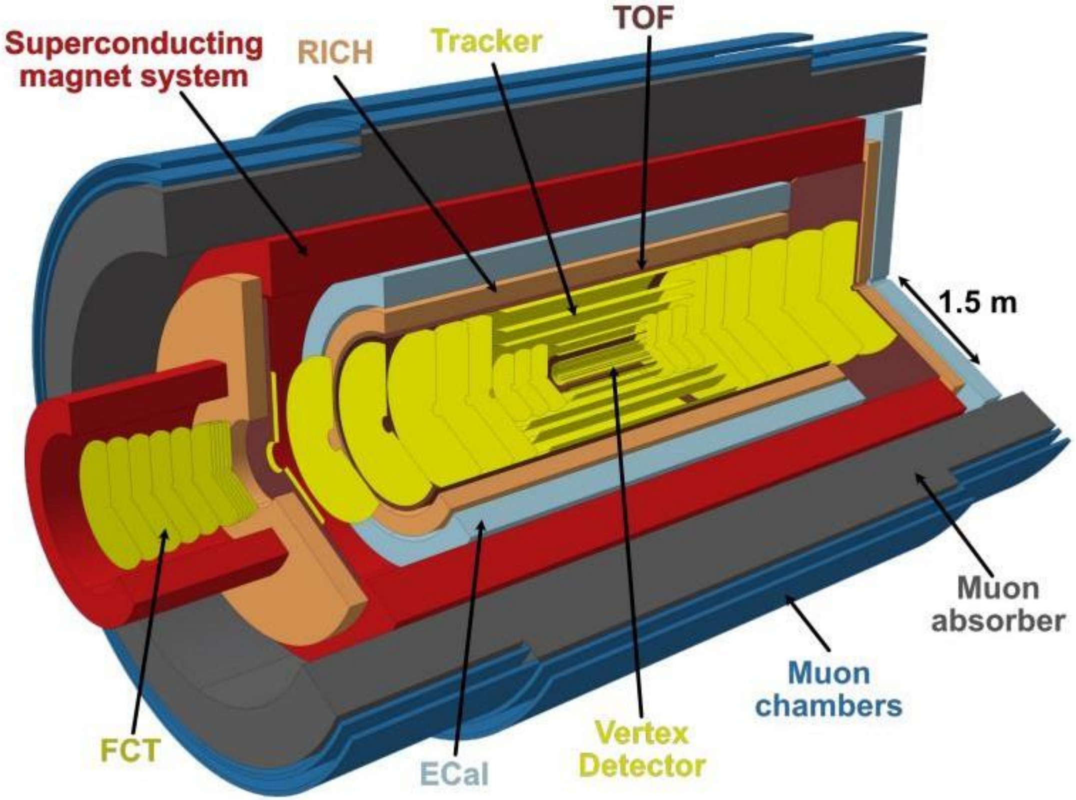




Transition to High Luminosity LHC

ALICE 3 LoI: CERN-LHCC-2022-009

	Pixels
Hybrid	• ATLAS ITk – Pixels • CMS Pixel Detector • LHCb VELO
Monolithic	• ALICE ITS 3, **ALICE 3** • LHCb Mighty Tracker & UP



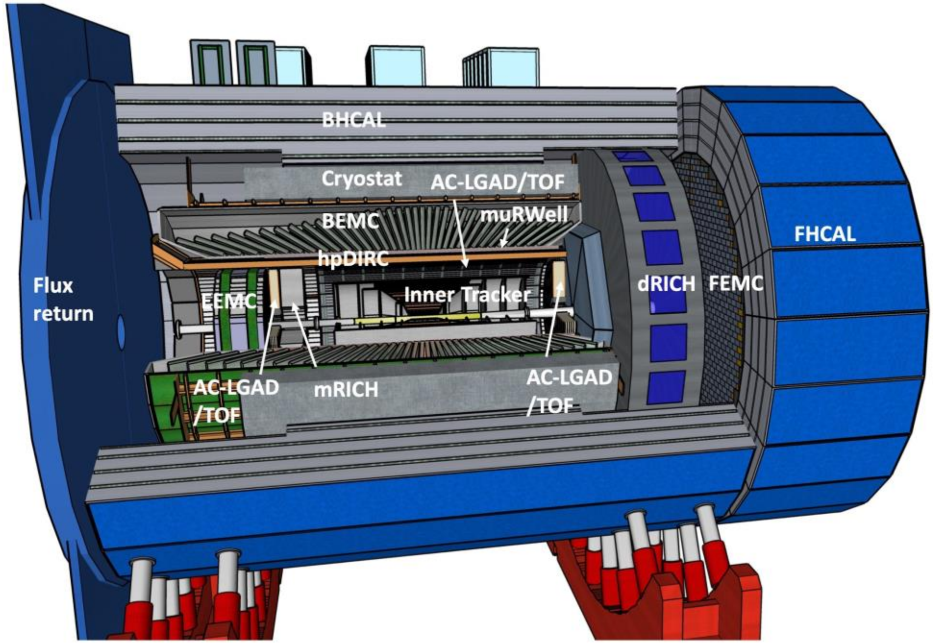
ALICE 3 – Very ambitious specs!

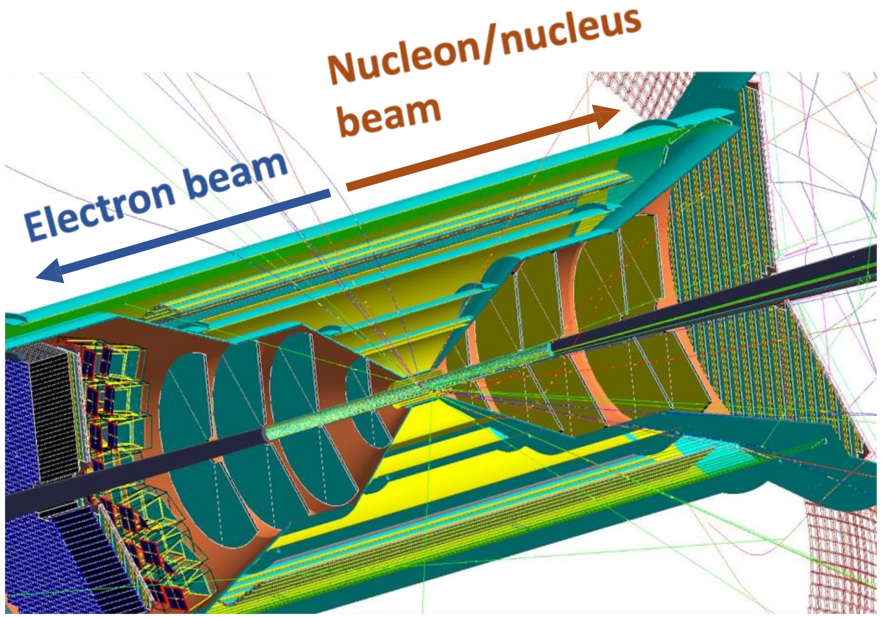
Process 65 nm CMOS (TPSCo)
Spatial resolution ~2.5 µm (vertex), 10 µm (tracker)
Low material budget 0.1% (vetex), 1% (tracker) per layer
TID 300 Mrad
NIEL e16 n_{eq}/cm^2
Power consumption ↓ mW/cm^2
Total area 60 m^2

- 3 layers of wafer-size, ultra-thin, curved, CMOS MAPS **inside the beam pipe** in secondary vacuum
- **Retractable** configuration thanks to **movable petals**: distance of **5 mm** from beam axis for data taking and **16 mm** at beam injection

Non-LHC – EIC ePIC detector

- **Requirements for its silicon vertex and tracking detectors**
  - Pixel size ~10 µm
  - Material budget 0.05% X/X0 per layer
  - Time resolution O(100 ns)
  - Fake-hit rate <e-7
  - Radiation tolerance ~e15 n_{eq}/cm^2 at 20 °C





In line with ALICE ITS3 sensor specifications (+ similar timeline)

EIC detector based on ITS3 65 nm CMOS sensor (with stitched staves)

Other non-LHC experiments

- **Mu3e Phase I: first application of monolithic HV-CMOS in an experiment**
  - Low material 50 µm
  - Good time resolution < 20 ns (for pixels)
  - Fine segmentation 80 µm x 80 µm
- **Mu3e Phase II:**
  - Will require much improved timing
- **KOTO-II at JPARC (flavour physics at fixed target programme):**
  - Plans to develop and deliver novel silicon detectors for its tracker

FCC-ee

- **Requirements for its silicon vertex and tracking detectors**
  - Small pixel size for high precision
  - Low mass
  - Low power
  - Moderate radiation tolerance
  - Large area coverage
- **Other e+e- colliders**
  - Similar technology requirements

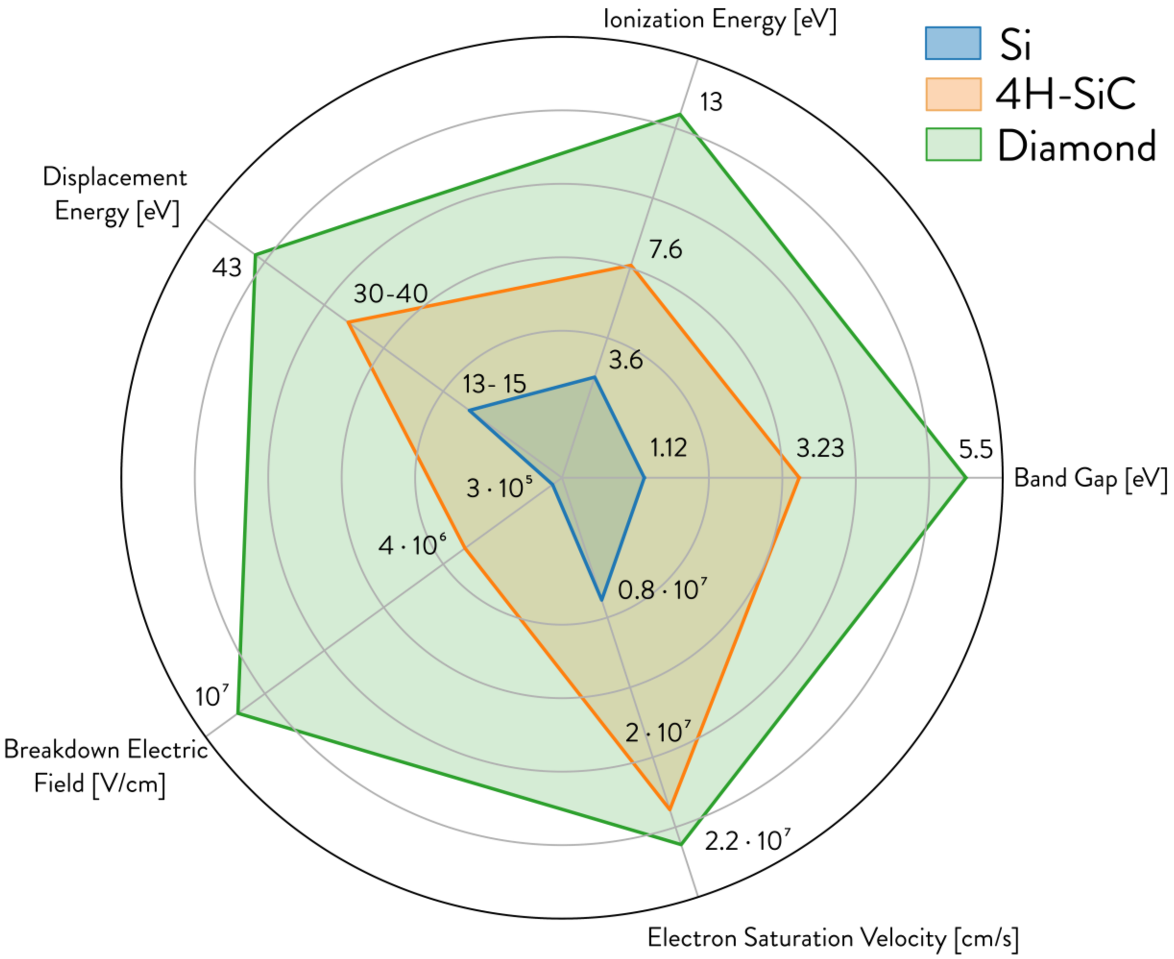
FCC-hh

How will technology look like in 50 years time?

- FCC-hh will require even more advanced radiation tolerant detectors than the LHC experiments.

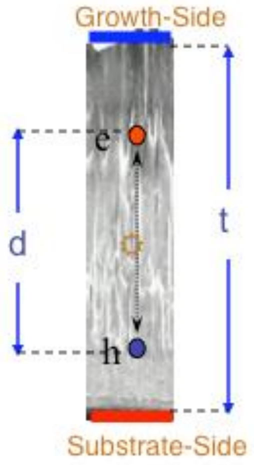
Wide Bandgap materials

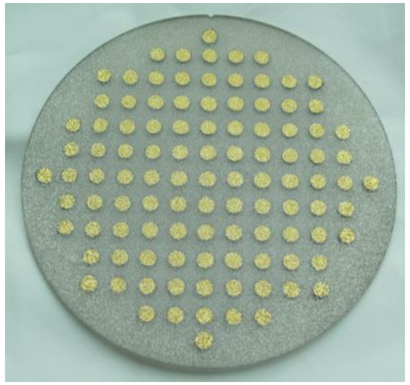
- **Input from**
  - RD42
  - RD50
  - DRD3-WG6
- **Diamond**
  - Well established
  - Used at LHC (ATLAS, CMS)
- **SiC**
  - Very attractive developments in RD50/DRD3
- **GaN**
  - At an early stage

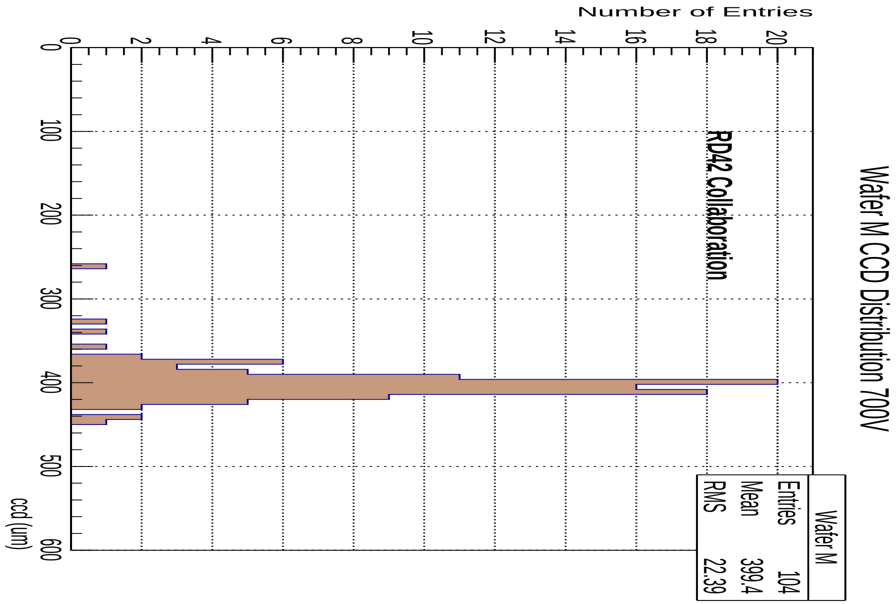


CVD diamond – Development goals

- Removal of surface defects
  - few per cm^2 → **< 1 per cm^2**
- Wafer charge collection distance (d) in pCVD
  - 400 µm → **500 µm**
- Size of wafers = 15 cm (6 inch) diameter state-of-art fixed by microwave frequency (not expected to change)
- Wafer uniformity
  - 5% → **2% across whole wafer**
- Price per cm^2
  - ~1500 USD/cm^2 → **800 USD/cm^2**



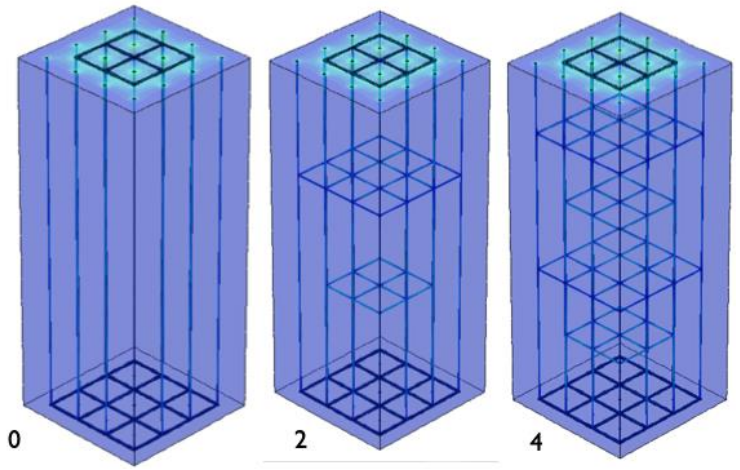


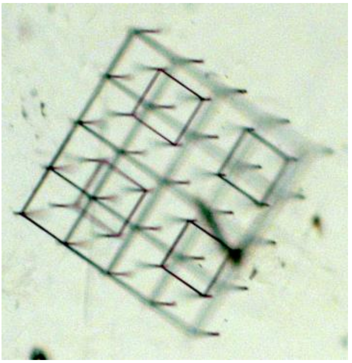


3D diamond detectors – Possible FCC devices

- 3D seems to be a viable option to enhance radiation tolerance
- Radiation hardness requirement and resulting Schubweg dictate cell size
- Cell size determined by wire-diameter (1 mm) and cell capacitance
- $(25mm)^2$ or even below seems feasible
  - Loss of efficiency small at 10^{17} peq
  - $25 \div 2 \times \sqrt{2} = 18$ mm drift path vs λ = 18 mm

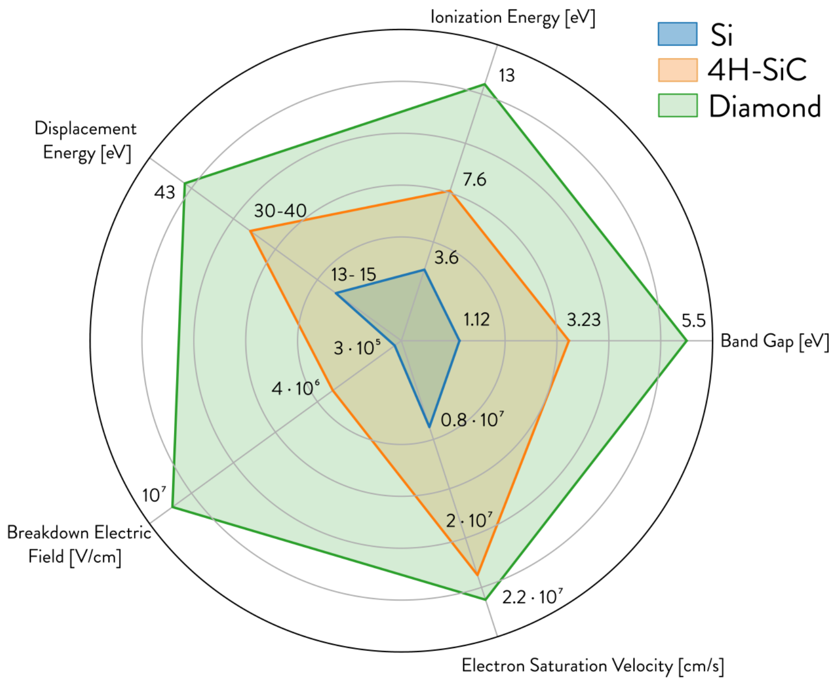
  Leakage current not an issue
- Main technological challenge for large scale application is the scaling of wire production





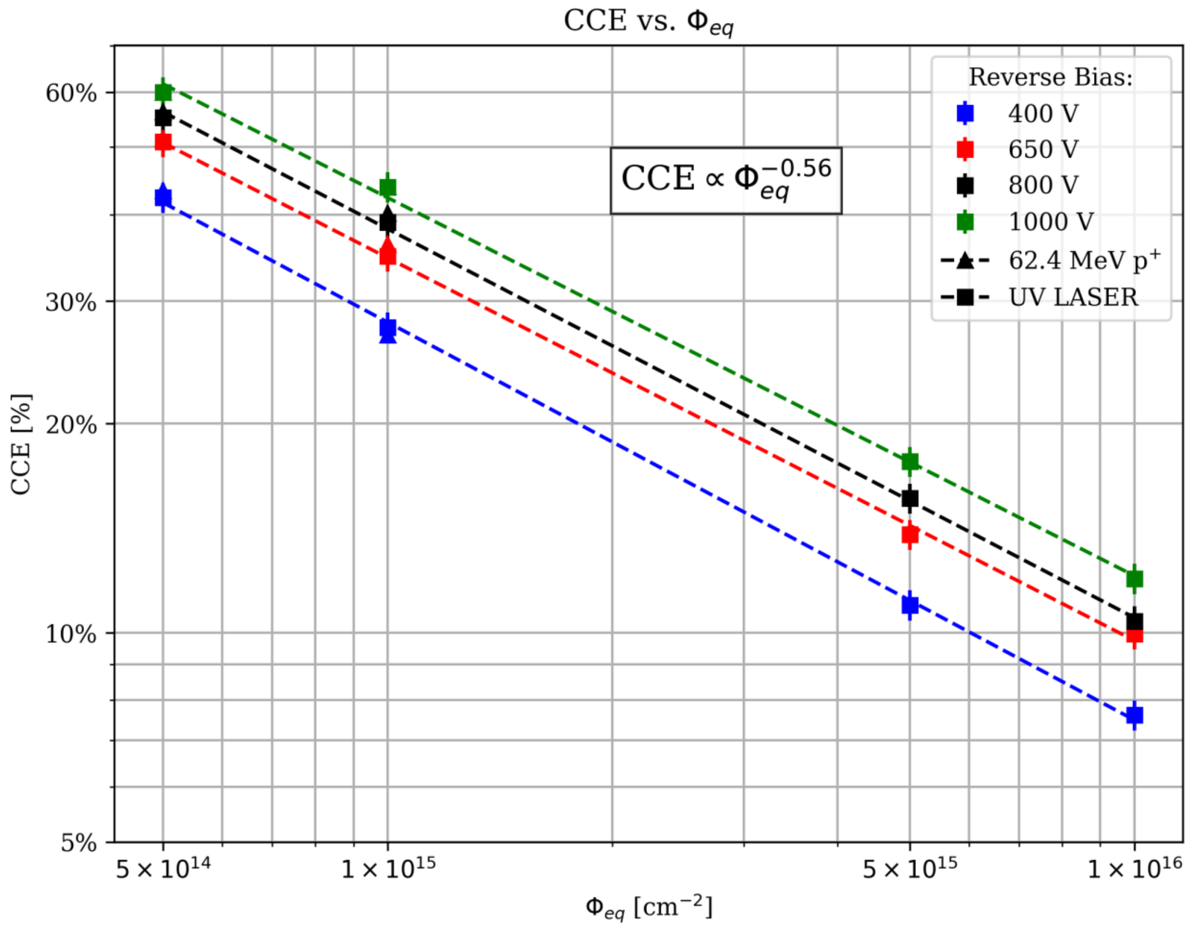
SiC status

Physical Parameter	Si	4H-SiC
Band gap energy [eV]	1.12	3.26
Thermal conductivity [W/K·cm]	1.5	4.9
Breakdown field [MV/cm]	0.3	3.0
Electron saturation drift velocity (cm/s)	1×10^7	2×10^7
Hole saturation drift velocity (cm/s)	0.6×10^7	1.8×10^7
Mean ionization energy for e/h pair (eV)	3.6	7.8
Atomic shift threshold energy(eV)	13	22



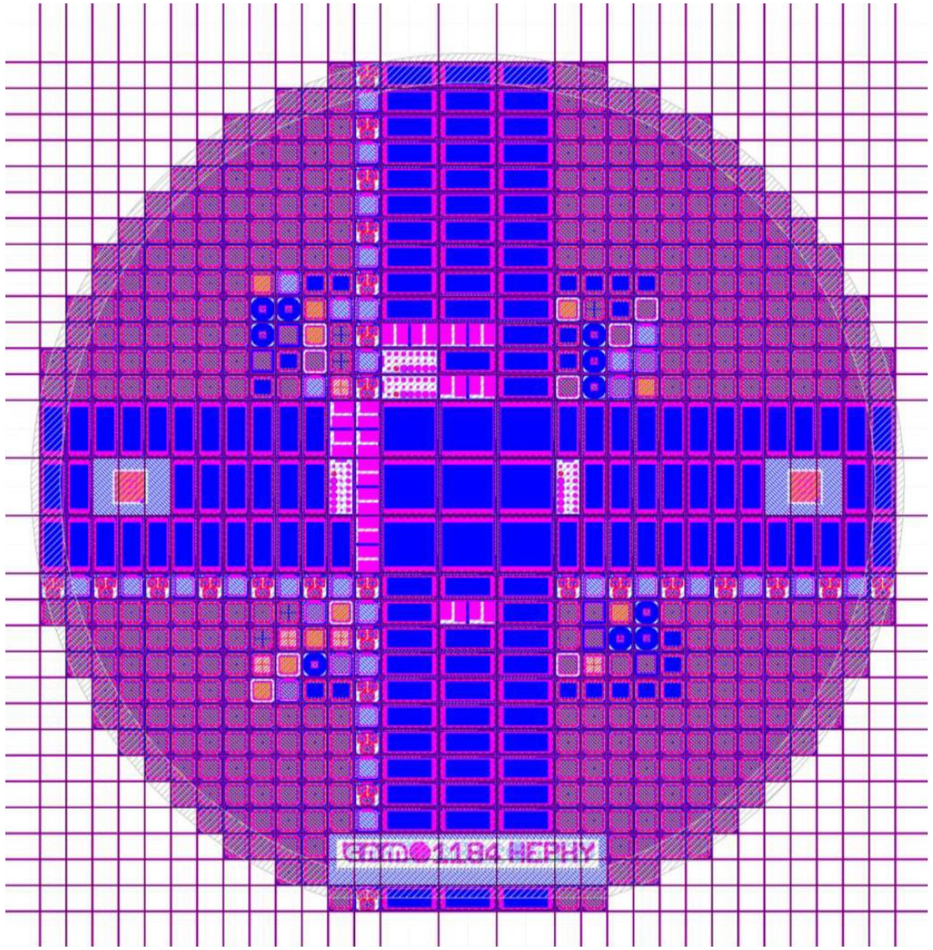
SiC status: radiation tolerance

- CCE follows a power law ($\propto \Phi^{-0.56}$), even for different bias voltages
- CCE > 10% for $1 \cdot 10^{16}$ n_{eq}/cm^2
- More work needed to increase radiation hardness of SiC:
  - Annealing
  - Defect engineering



SiC status: planar 4H-SiC wafer-run

- In collaboration with CNM
- 3 x 50 µm & 2 x 100 µm active thickness
- Design at HEPHY, processing at CNM
- First samples are being tested
- Includes:
  - Pad & strip detectors, resistive detectors
  - Diodes for edge-TCT
  - Pixel array
  - MOSCAPs & MOSFETs (various forms and sizes)
  - Gate controlled diodes
  - Test structures (van der Pauw, Kelvin-bridge…)



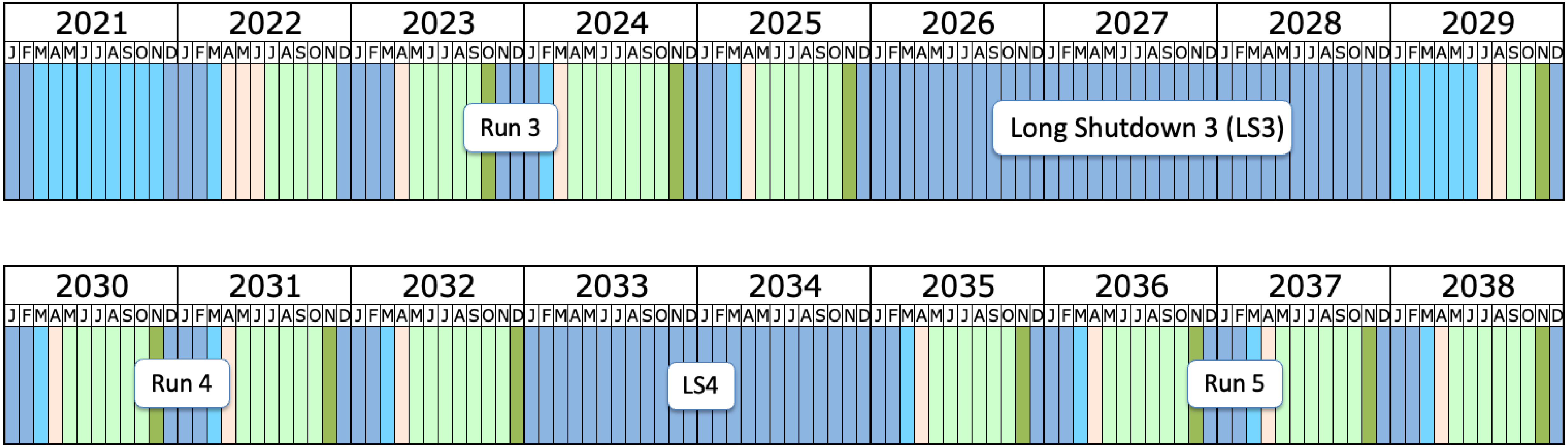
Conclusion

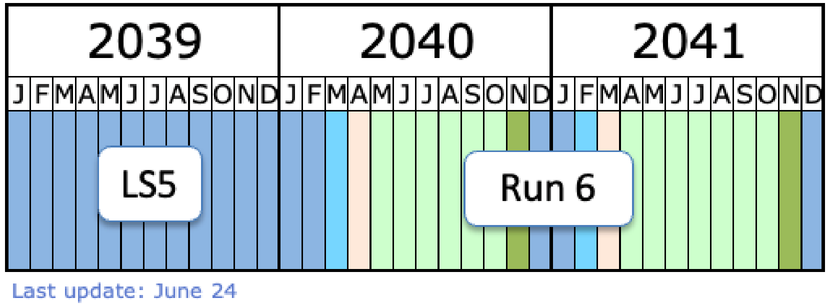
- **Solid-state sensors are everywhere in physics experiments**
- **Many cutting-edge technologies developed already fit for present experiments**
- **Several challenges ahead in view of future experiments**
  - High spatial resolution
  - High radiation tolerance
  - Zero mass
  - Fully integrated with electronics, mechanics, services
  - Large area sensors at low cost
- **R&D programme to develop new technologies and get us there**

Back up slides

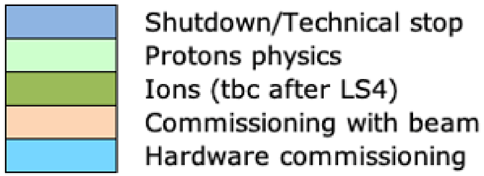
Longer term LHC schedule

Run 1 = 2011-12
Run 2 = 2015-18





From:
https://lhc-commissioning.web.cern.ch/schedule/LHC-long-term.htm



Longer term ALICE schedule