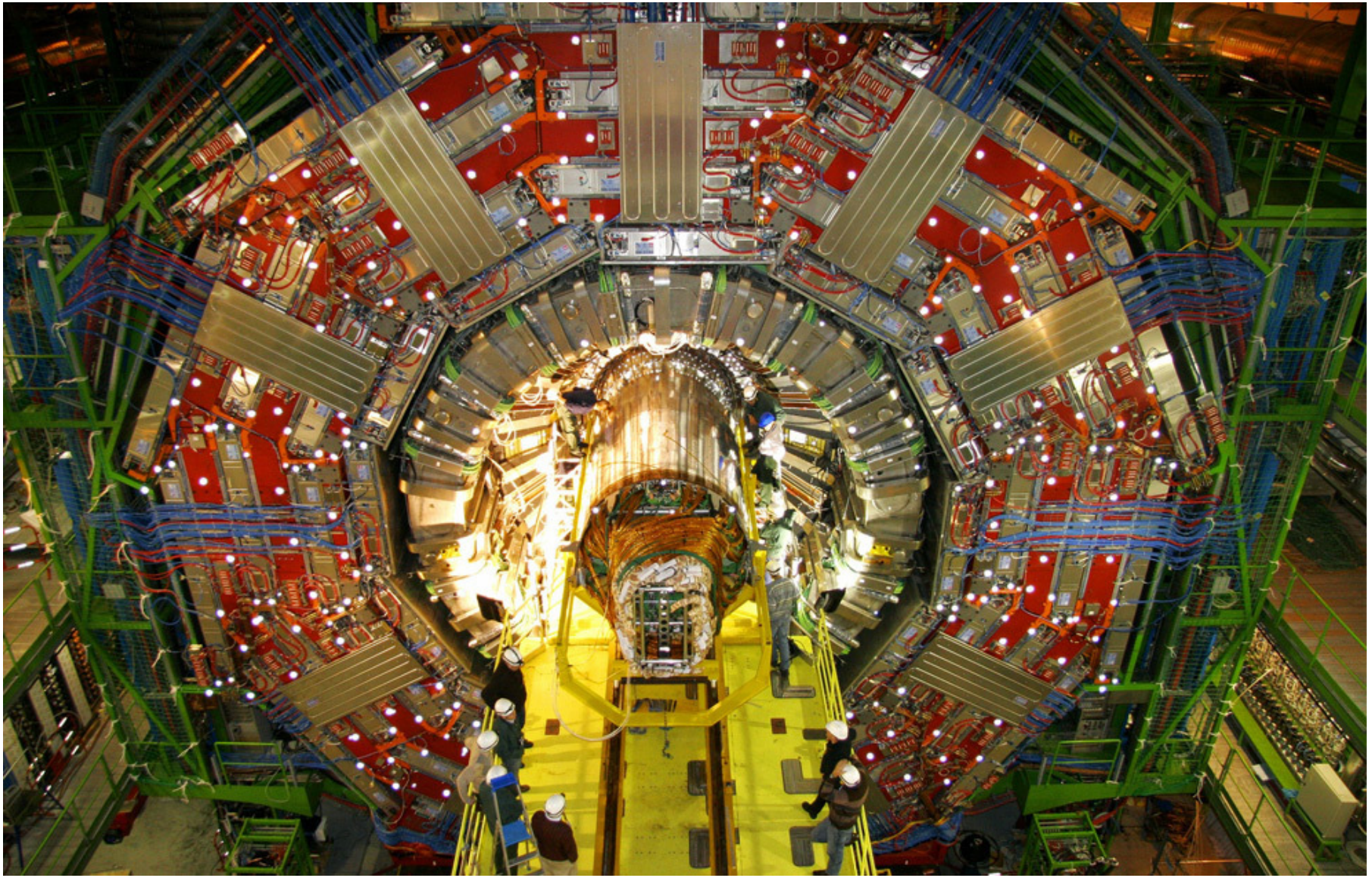
CMS Tracker Readout: Present and Future



outline

LHC

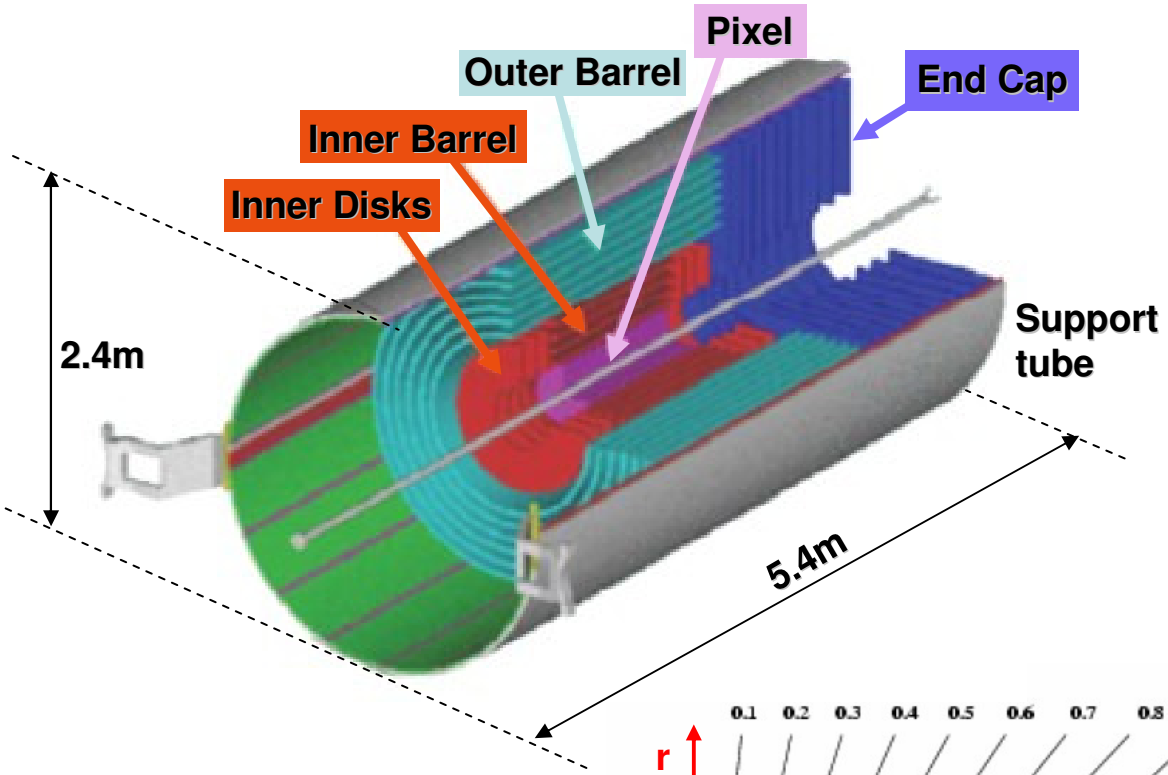
review of current CMS microstrip tracker
focus on readout architecture and front end chip (APV25)

SLHC

the challenges: power and triggering
prototype front end chip for short strips (CBC)
possible triggering architectures and tracker layout

will skip many details and neglect pixels altogether

CMS LHC strip tracker



some numbers

~ 200 m^2 sensor area

~ 15,000 detector modules altogether
22 different types

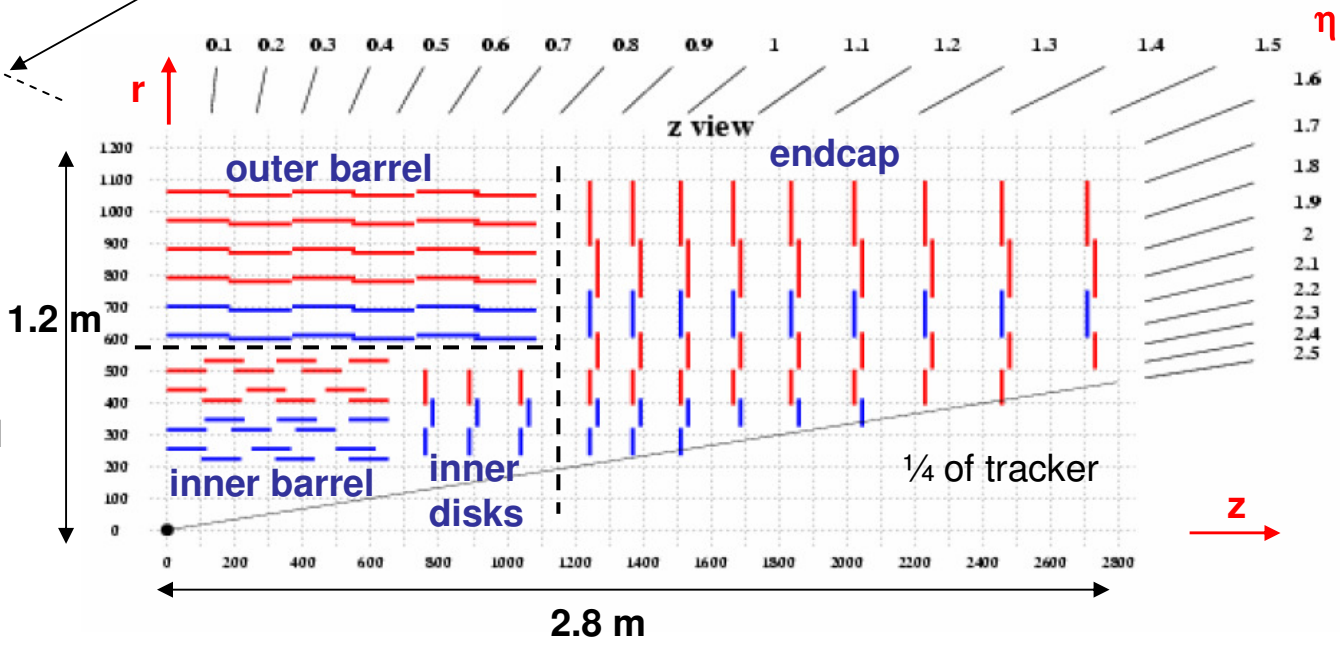
~ 10^7 strips, ~75,000 FE chips (APV25)

all single sided sensors

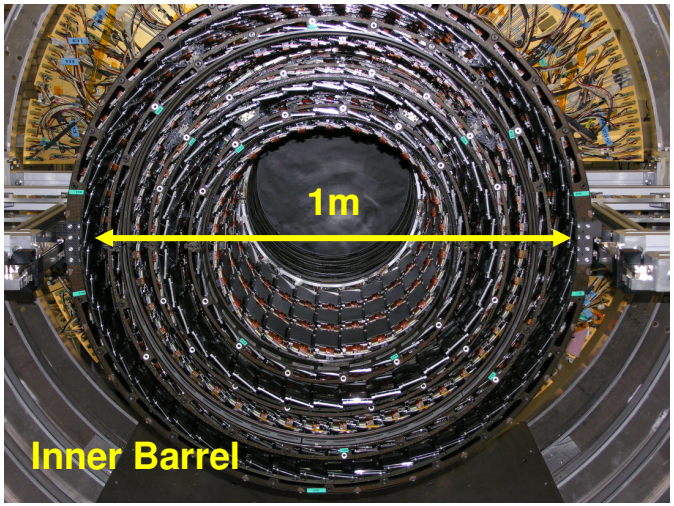
single layer modules

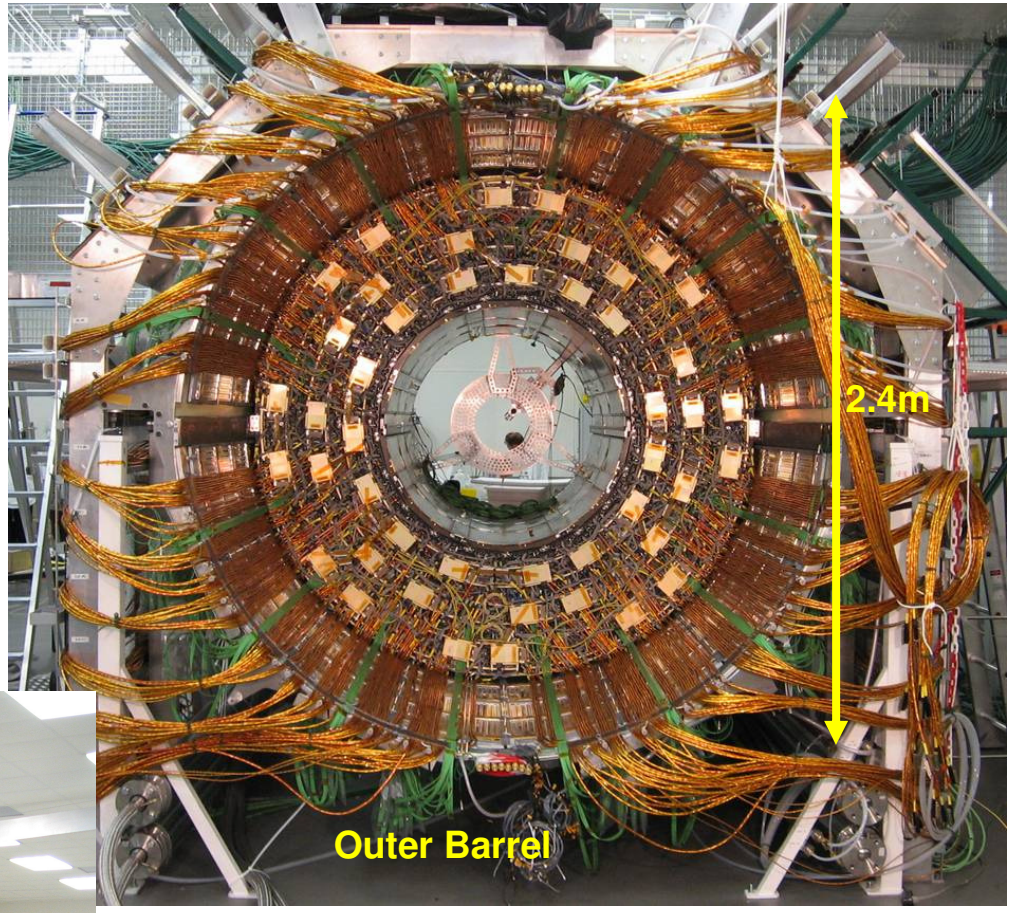
stereo modules

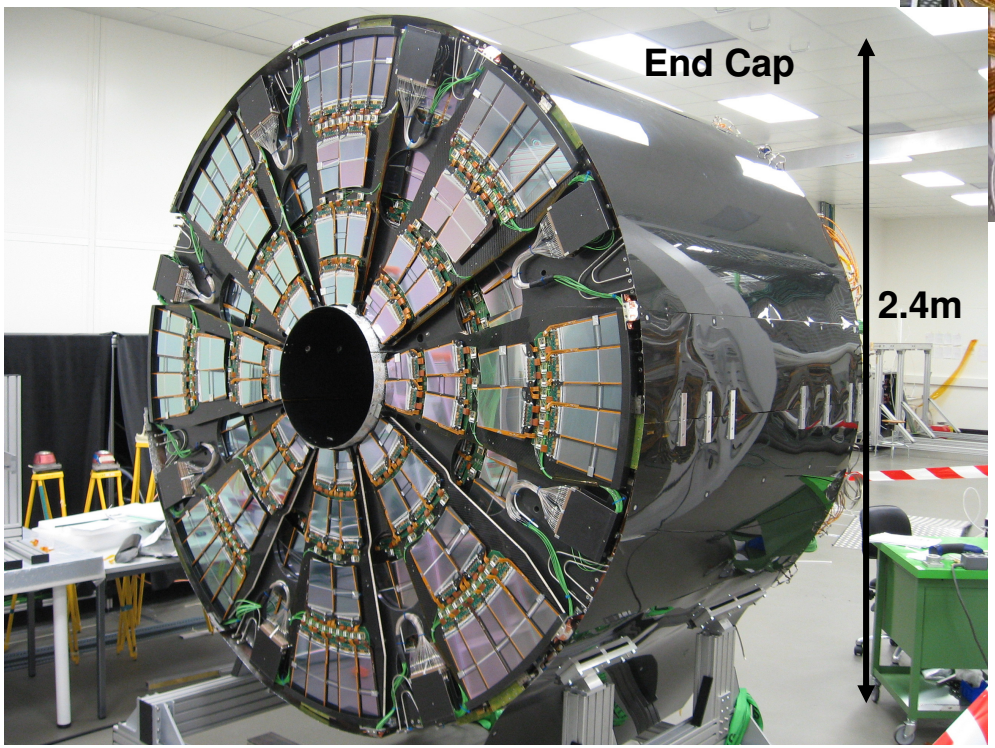
(stereo module = 2 single-sided modules closely spaced with angle between strips)



sub-detectors





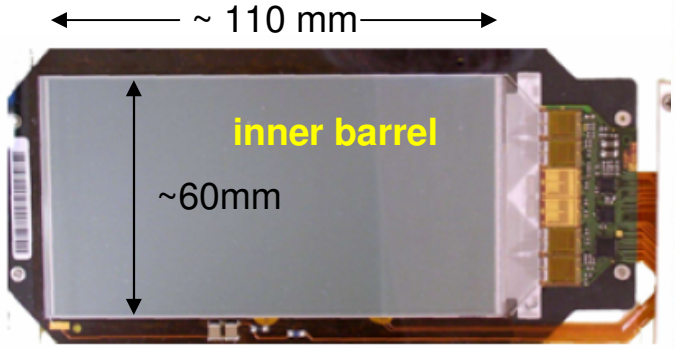


inner barrel
4 layers, 2 stereo

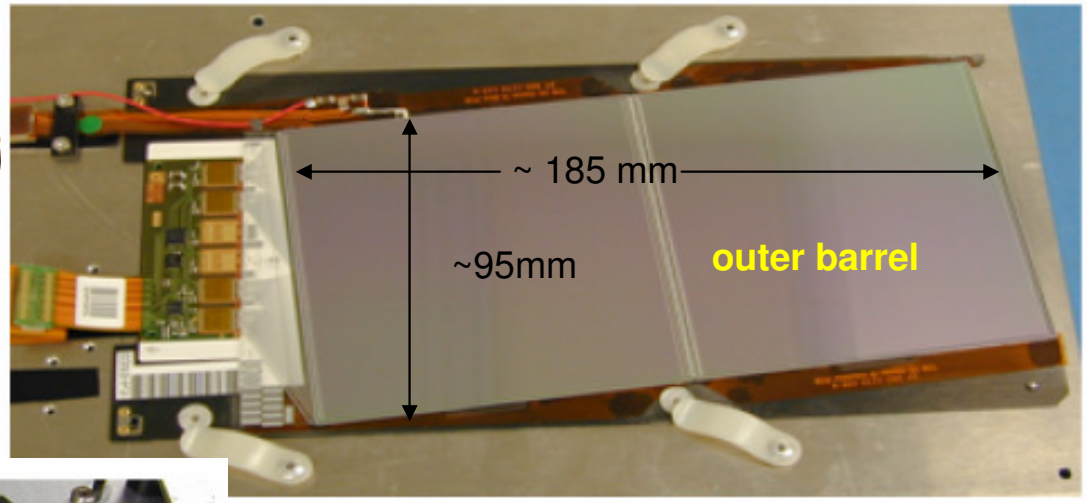
outer barrel
6 layers, 2 stereo

end caps
9 disks / endcap
mixture of single/stereo modules

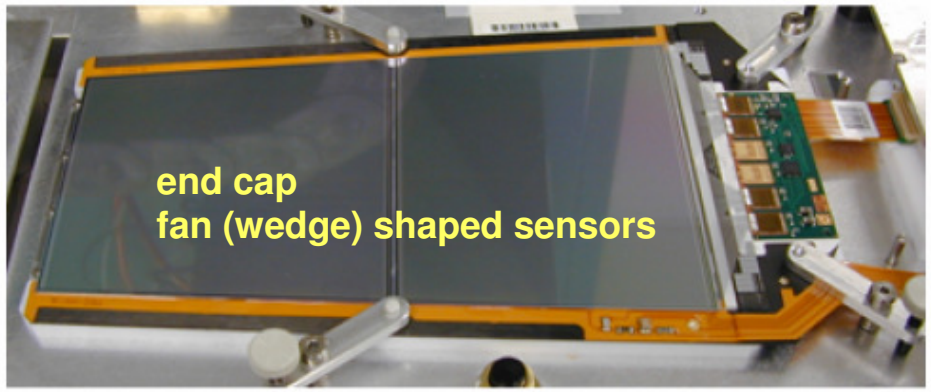
modules



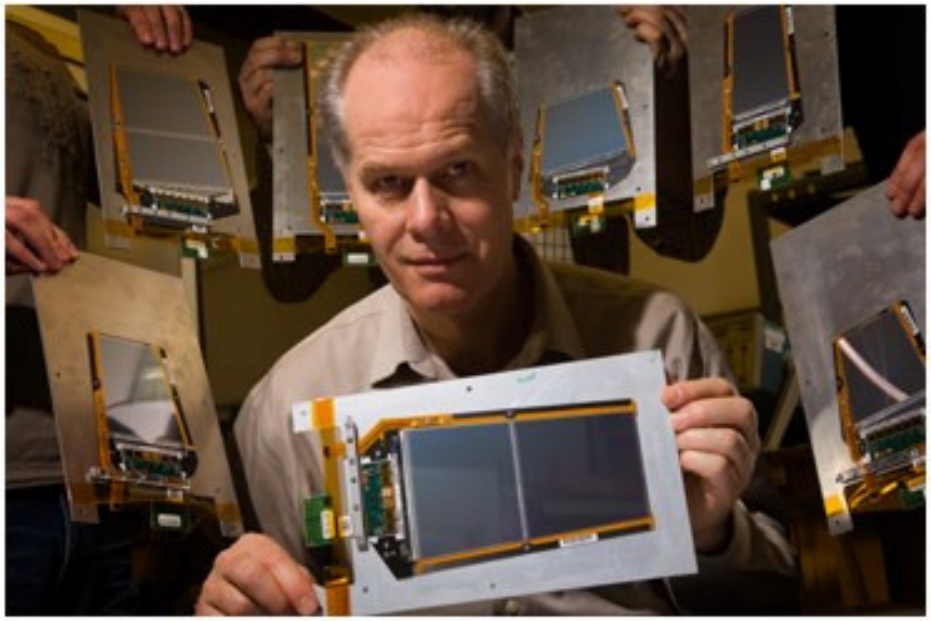
single sensor / module



double sensor modules



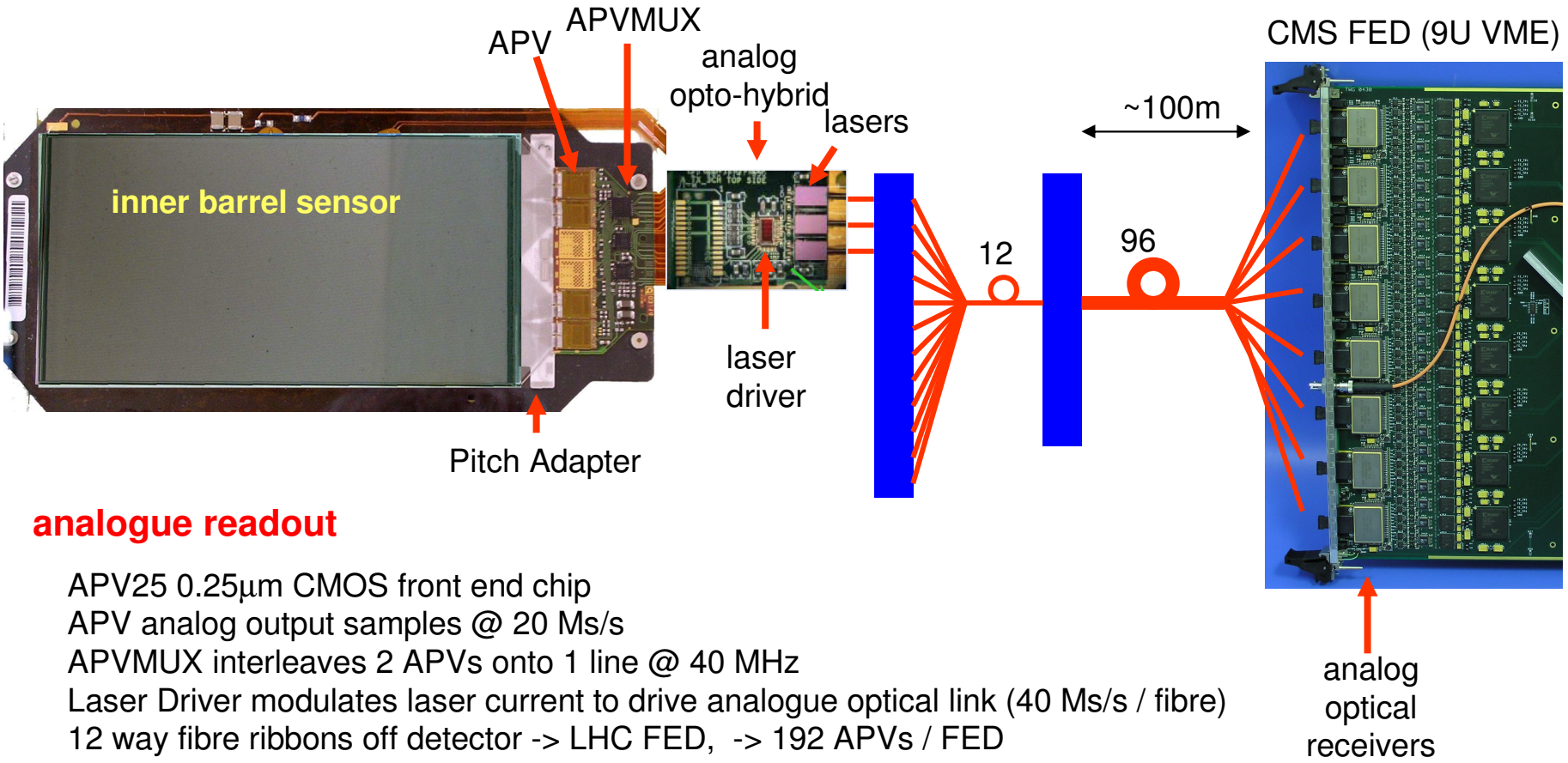
double sensor module



inner barrel
320 μm thick, 80/120 μm pitch
outer barrel
500 μm thick, 120/180 μm pitch
end caps
mixture of 320/500, 80-200 μm pitch

-> lots of different module varieties, 22 varieties altogether (with hindsight - too many)

CMS LHC strip readout system

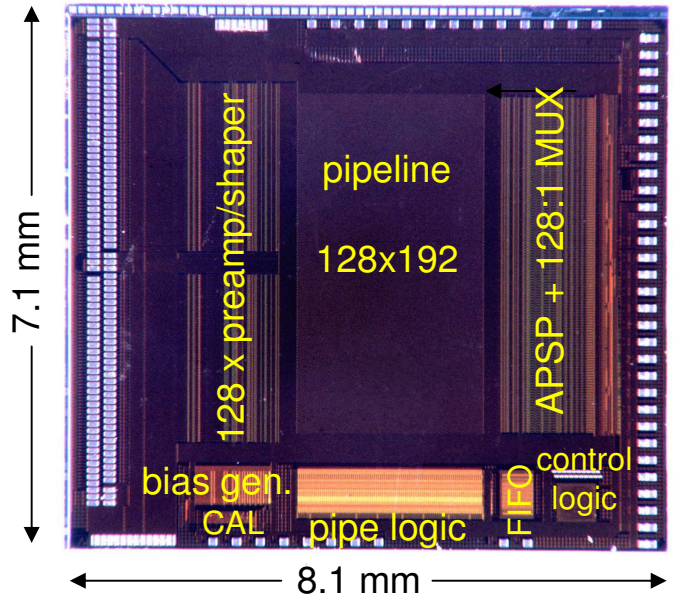


analogue readout

APV25 0.25µm CMOS front end chip
APV analog output samples @ 20 Ms/s
APVMUX interleaves 2 APVs onto 1 line @ 40 MHz
Laser Driver modulates laser current to drive analogue optical link (40 Ms/s / fibre)
12 way fibre ribbons off detector -> LHC FED, -> 192 APVs / FED
O/E conversion on FED and digitization
~ 9 bits effective => 360 Mbps

all on-detector chips in 0.25µm CMOS (including control system)
UK responsible for delivering front end APVs and 440 backend FEDs
a success for RAL microelectronics and systems

APV25



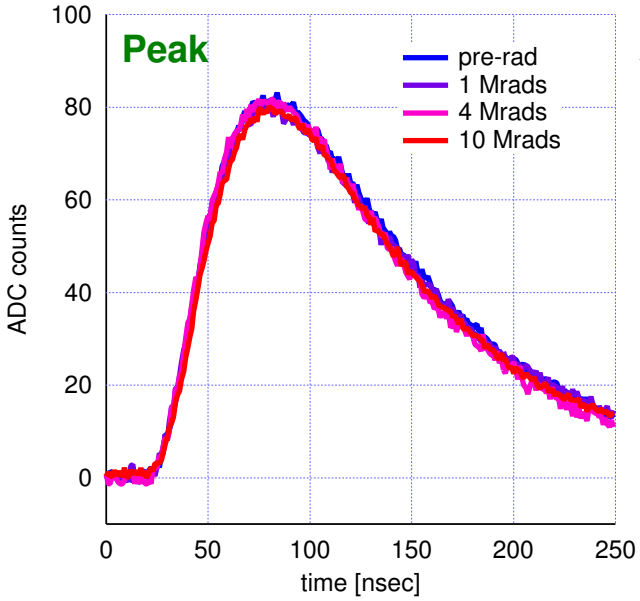
128 channel chip for AC coupled sensors
up to ~ 25 pF (long strips)

slow 50 nsec. CR-RC front end -> analogue pipeline
up to 4 μs L1 trigger latency

pipeline read out using **deconvolution** circuit
weighted sum of 3 consecutive time samples
gives single BX resolution

power: 2.7 mW / channel

rad-hard: >10 Mrads

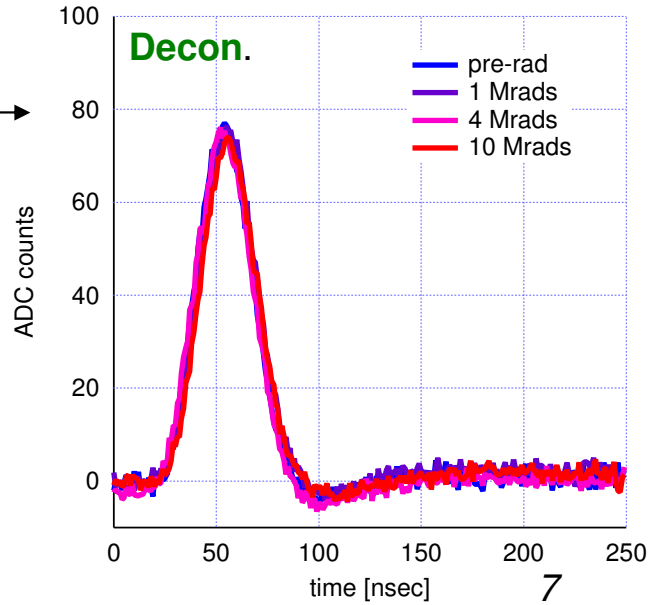


noise
270 + 38 e/pF (peak)
430 + 61 e/pF (deconvolution)

measured module S/N values (in final system)

thin sensors
(inner barrel, end caps)
~28 peak, ~19 decon.

thick sensors
(outer barrel, endcaps)
~35 peak, ~23 decon.



historical

For **LHC** radiation hardness was the big issue

power was also an issue
- original goal 2 mW / channel (we didn't manage it)

APV development had roots in **RD20**
- generic R&D into sensors, electronics & mechanics (cooling, materials) for LHC

much of FE electronic R&D in the 90's concentrated on investigating rad-hard processes
- e.g. Harris, DMILL,… - feature sizes ~ 1 μm

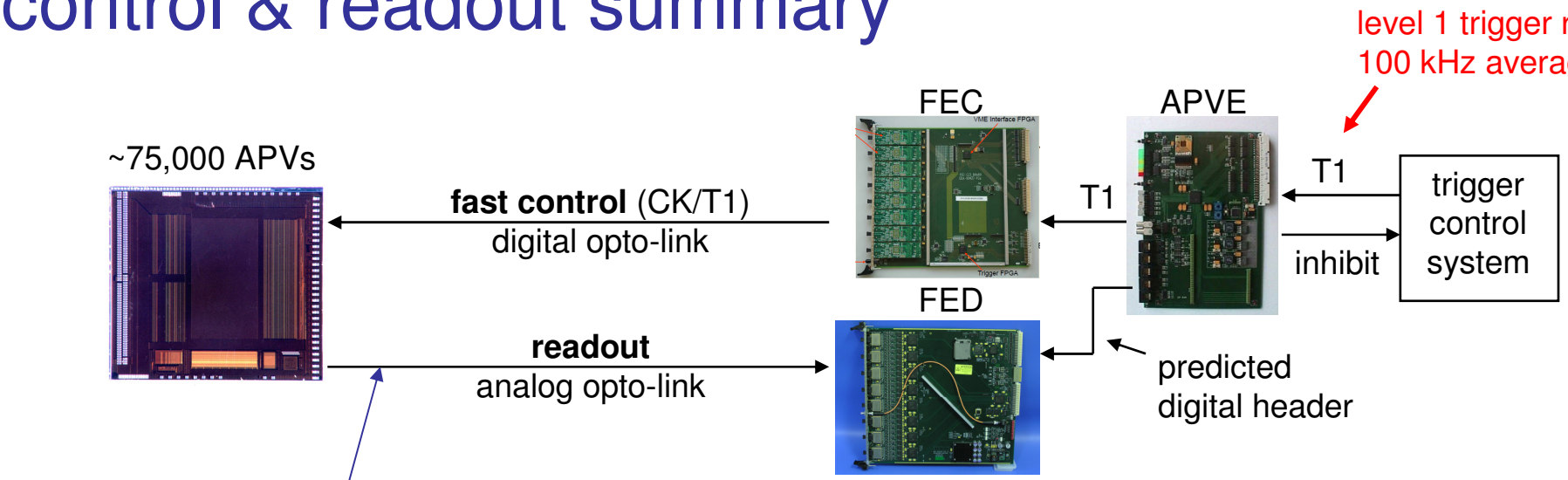
0.25 μm CMOS turned up just in time for CMS (~1998)
- very rad-hard (thin gate oxide)
- APV25 developed in ~ 2 years
  - major success for UK (RAL Microelectronics)

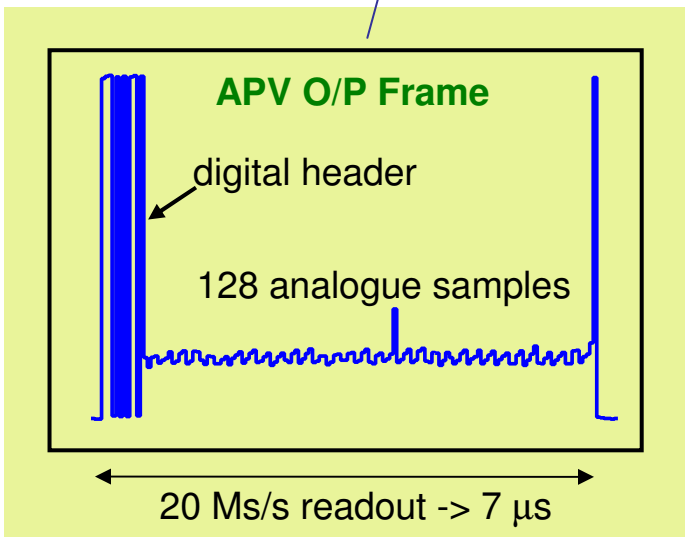
For **SLHC** radiation hardness of less concern
- **0.13 μm** now available to us: ionizing ok, SEU will need care

APV development history

1992	amplifier and transistor test structures in Harris
1993	**APV3** – 32 chans preamp/shaper/pipeline/APSP
1994/5	**APV5** – 128 channels + mux
1996	**APV6** – APV5 + bias generator + I2C interface
1997/8	**APVD** – DMILL version
1998	**APVM** – APV6 version for MSGCs
1999	**APV25s0** – 1st 0.25 μm version
2000	**APV25s1** – final version – the one we use today
2001	volume production launched
2002	low yield problems – long story eventually understood and process tweaked
2003	volume production resumed ~ 85% average yield
2005	production finished

control & readout summary





no zero-suppression (no sparsification) on detector

all 75,000 APVs operating synchronously
(all FE chips doing same thing at same time)

advantages

can be emulated externally (APVE) to prevent
APV buffer overflows
easy to identify upset chips (digital header)

pedestal, CM subtraction and zero suppression on FED

raw data also available for setup, performance monitoring and fault diagnosis

analog, unsparsified readout provides relatively simple and robust system

SLHC

timescale

~**2017** - Phase I - new pixel detector
4 layers
new readout electronics
based on existing architecture but some modifications and scaling
lighter, CO2 cooled

~**2021** - Phase II - complete new tracker

CMS strip tracker for phase II

the challenges

1) power

higher granularity (shorter strips) => more FE chips
electronics related material dominates existing material budget (cabling, cooling) & we want to reduce this
consumption: technology helps but # of channels increases
delivery: constrained by existing cables - need to bring in at higher voltage => DC-DC conversion or serial powering
CMS has chosen DC-DC as baseline

2) triggering

not possible to keep L1 trigger rate at 100 kHz without info from tracker

=> new features and new architectures needed

what we like about our present system

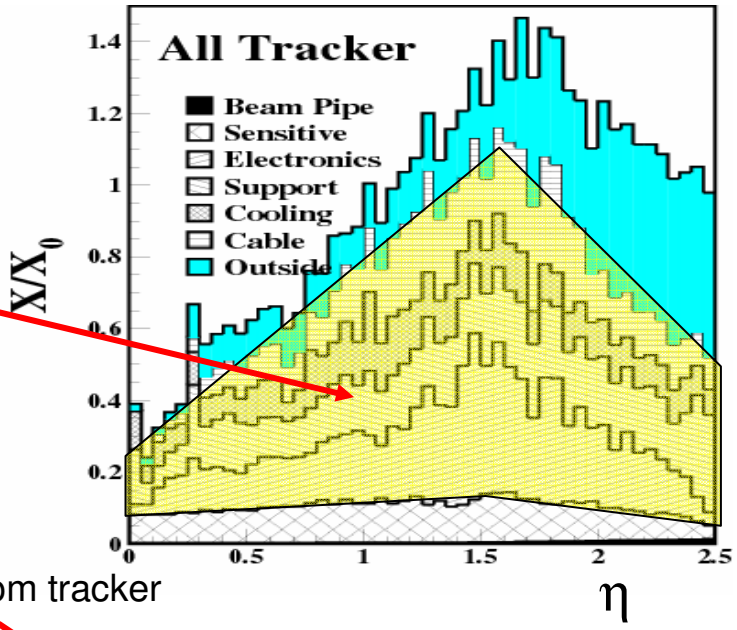
analog pulse height info - made possible by custom analog link
system simplicity - no on-detector sparsification
-> occupancy independent data volume

what must change for SLHC

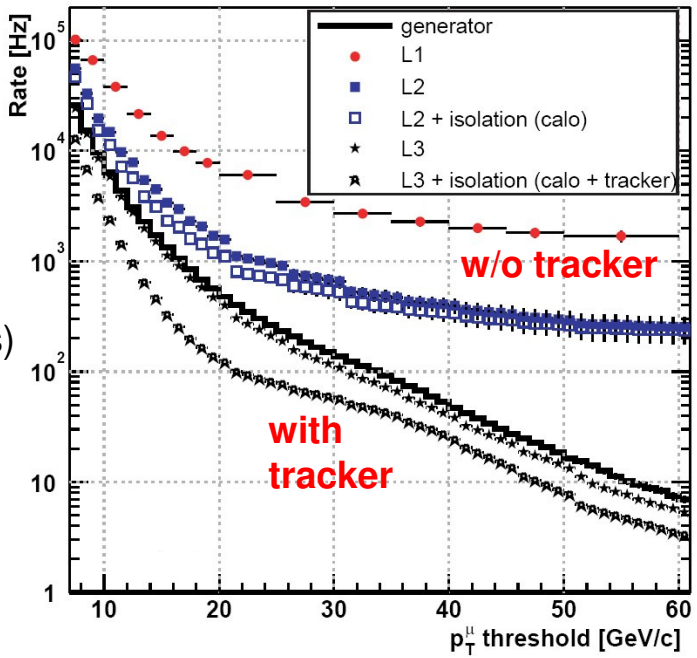
off-detector links -> high speed digital (follow commercial trends)
=> ADC on front end if want to retain pulse height info
=> large data volumes if don't want to sparsify

our choice is not to sparsify

CMS tracker material budget



L=10^{34} muon trigger rate



architecture choice

CBC

have chosen binary un-sparsified architecture

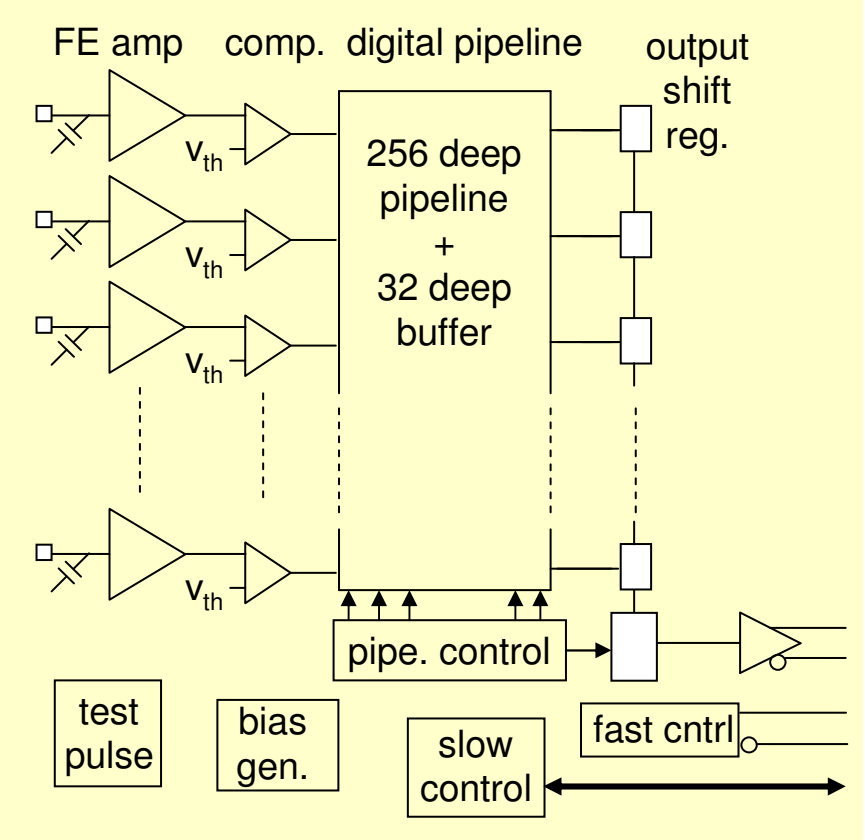
very simple, no ADC
=> low power
=> retain robust synchronous system

binary front end also compatible with possible triggering implementations (later)

=> CMS Binary Chip (CBC)

main features

- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- simple shift register output



CBC implementation

CBC produced in IBM 130 nm CMOS process

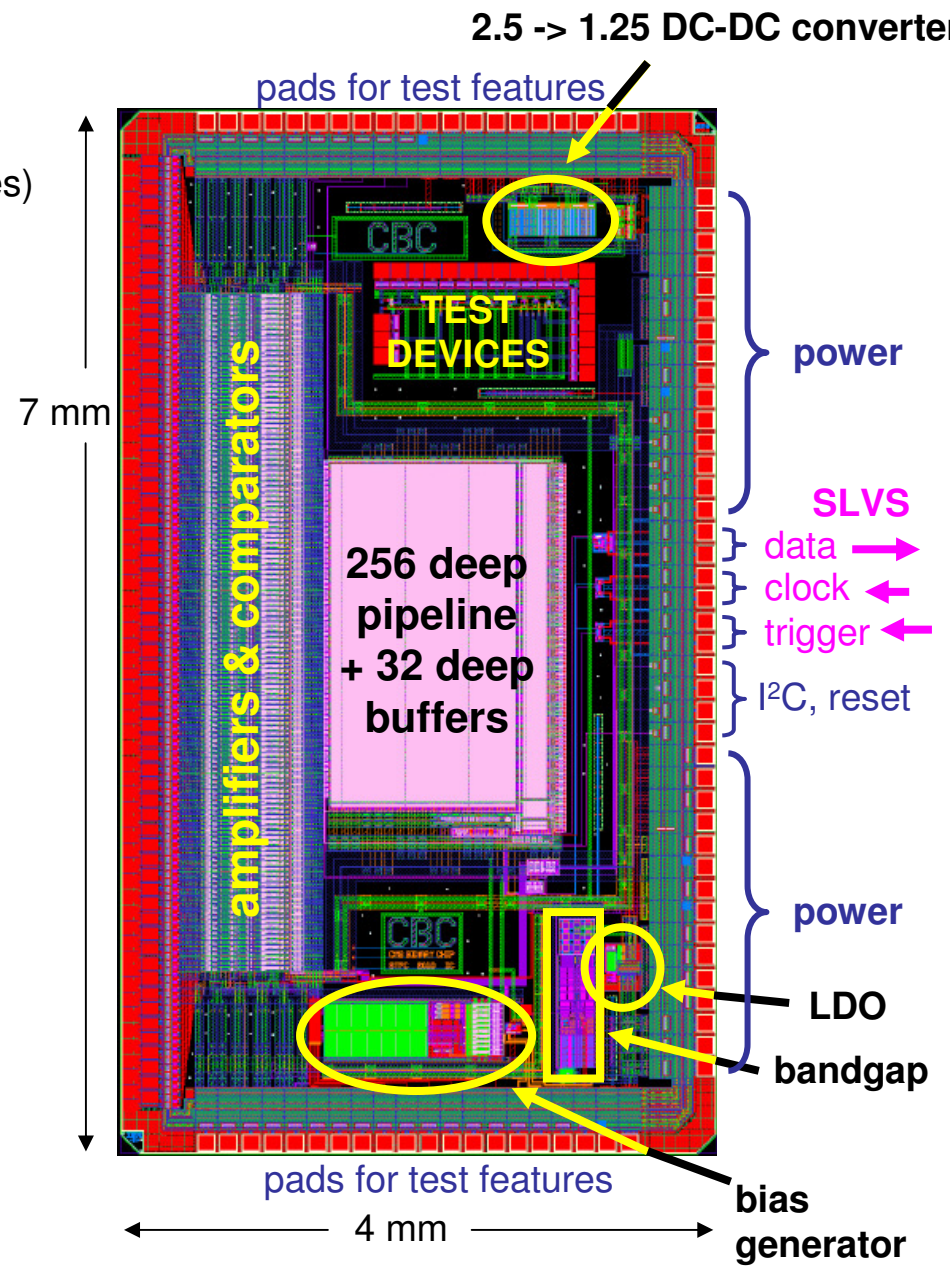
RAL/Imperial design - RAL layout (Lawrence Jones)
chips under test since Feb. 2011

key features

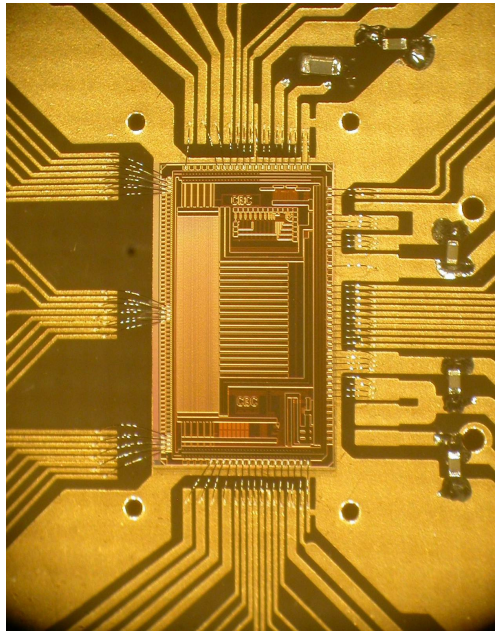
- designed for short strips, ~2.5 - 5cm, < ~ 10 pF
- full size prototype - 128 channels (50 μm pitch)
- not contributing to L1 trigger
  (can be adapted to 2-in-1 type triggering)
- powering test features
  2.5 -> 1.2 DC-DC converter
  (used in scenario where buck converter provides 2.5 V from 12 V rail)
  LDO regulator (1.2 -> 1.1) feeds analog FE
- fast (SLVS) and slow (I2C) control interfaces

some target specs

- DC coupling to sensor – up to 1 uA leakage
- can be used for both sensor polarities
- noise: < 1000e for C_{SENSOR} ~5 pF
- power consumption
  < 0.5 mW/channel for C_{SENSOR} ~ 5 pF



test setup



dummy channel
interface board
fast & slow control
& data out interface
test
charge
injection
CBC test board
~ 22 x 22 mm²
bias generator
test board

basic functionality

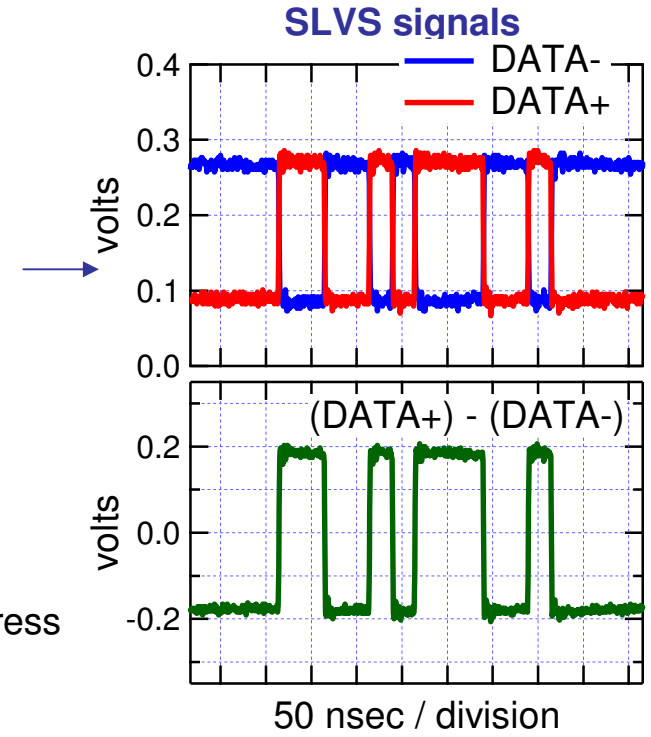
communication interfaces

fast: SLVS (Scalable Low Voltage Signalling)(CERN)
used for 40 MHz clock I/P, L1 trig and data out

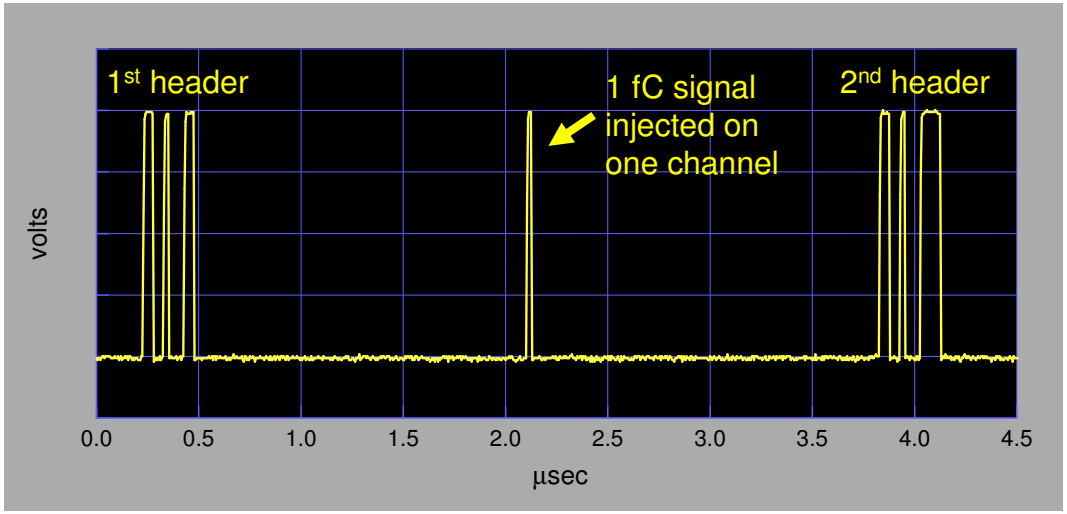
slow: I2C - used to programme
bias generator
operational modes, latency,..
128 comparator threshold trim values

output data frame

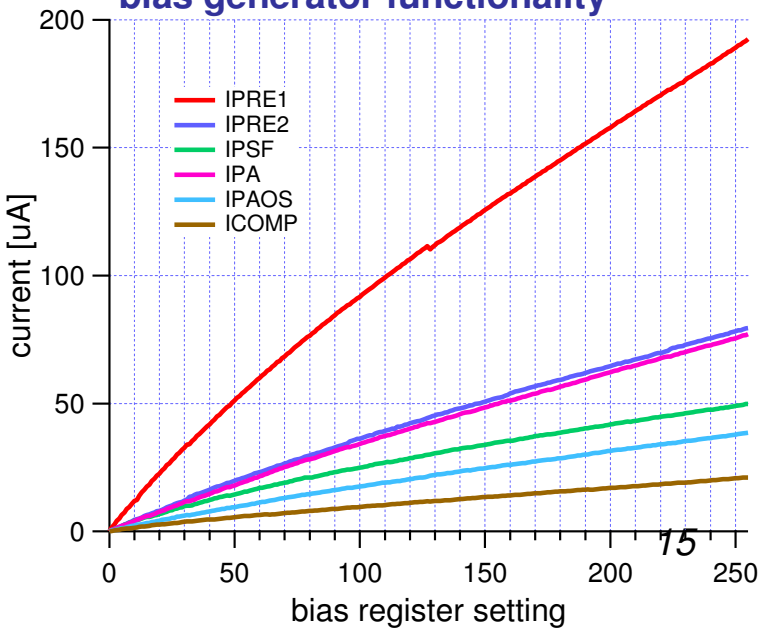
following trigger get 12-bit header
2 start bits, 2 error bits (latency, fifo overflow), 8 bit pipe address
followed by 128 channel bits



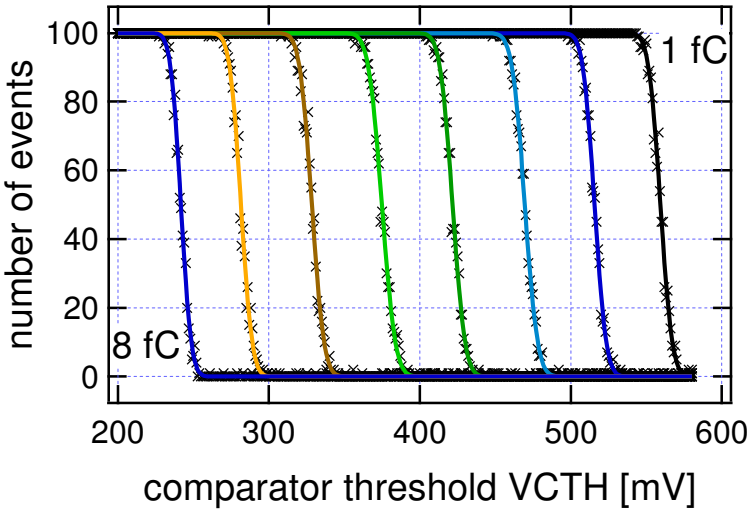
e.g. 2 consecutive data frames (2 triggers)



bias generator functionality

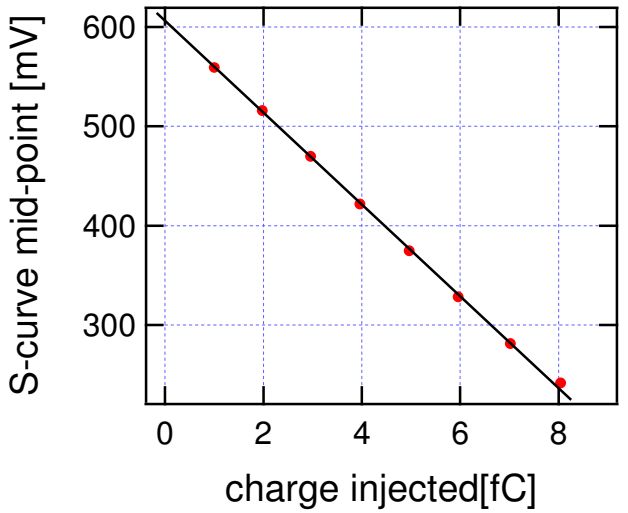


S-curves, gain & noise

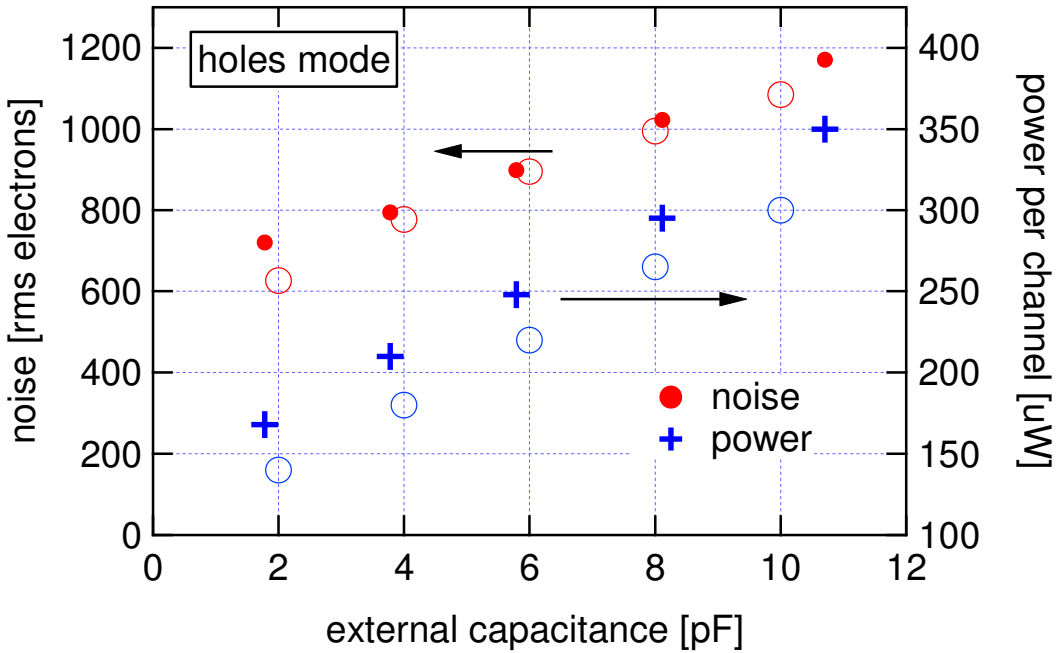


electrons mode
gain ~ 50 mV / fC
signals in range 1 - 8 fC
in 1 fC steps

gain



noise



noise and analogue power dependence on external added capacitance

current in input transistor adjusted to maintain pulse shape as external capacitance varies
- so overall analogue power varies

results very close to simulation (open circles)

target spec. < 1000e for 5 pF sensor

no sig. difference electrons or holes polarity

comparator threshold tuning

individual channel threshold tuning
128 registers, 8-bit precision

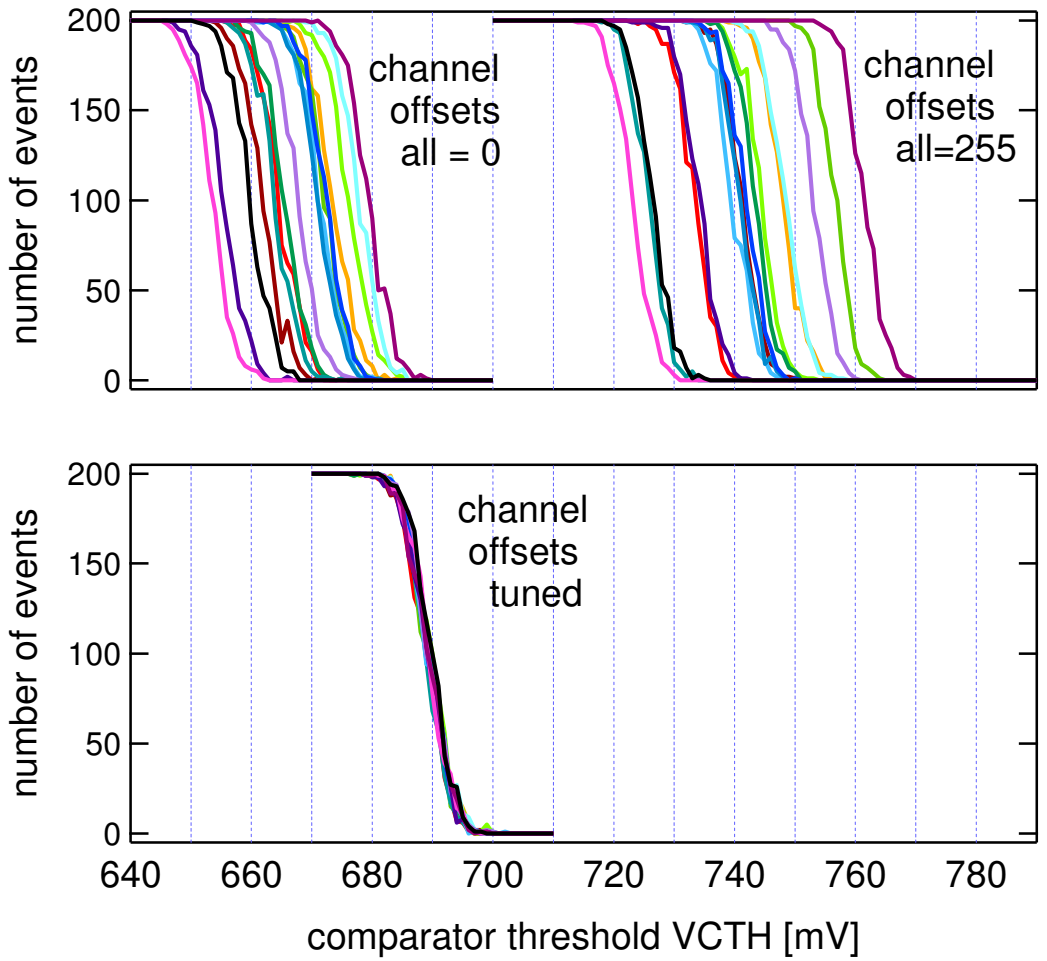
peak-to-peak threshold spread ~ 30 mV

< 1 fC (~50 mV) before tuning

pictures demonstrate effectiveness of tuning to achieve comp. threshold matching

~ mV precision achievable

threshold tuning - 16 channels



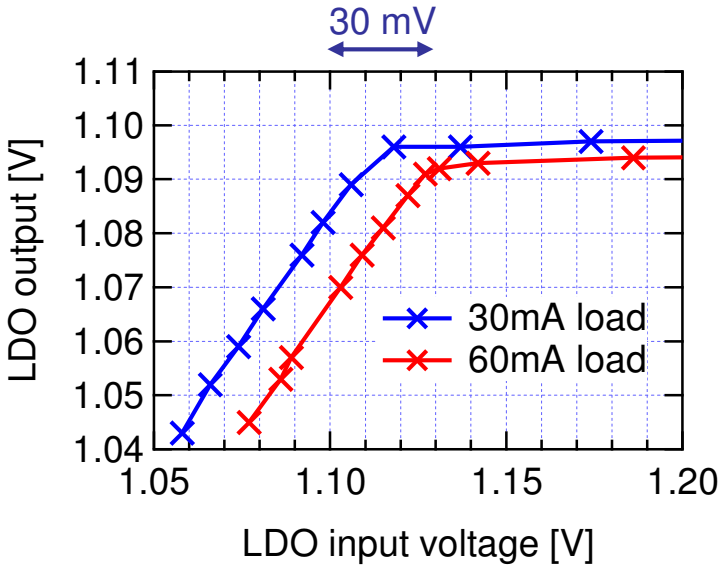
power circuits performance

DC measurements show LDO performing well

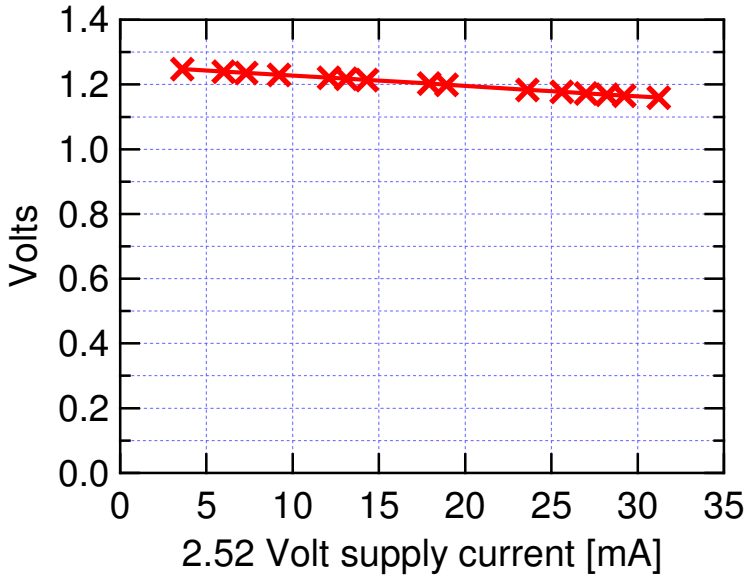
dropout = minimum difference between input and output before output starts to fall

only 30 mV for 60 mA load

LDO dropout



DC-DC output vs. load



efficiency measured for ~ nominal CBC load

2.52 V / 14.2 mA -> 1.2 V / 26.4 mA

=> ~ 90%

noise performance under study

power consumption

analogue

depends on sensor capacitance

130 + (21 x C_{SENSOR}[pF]) uW

digital

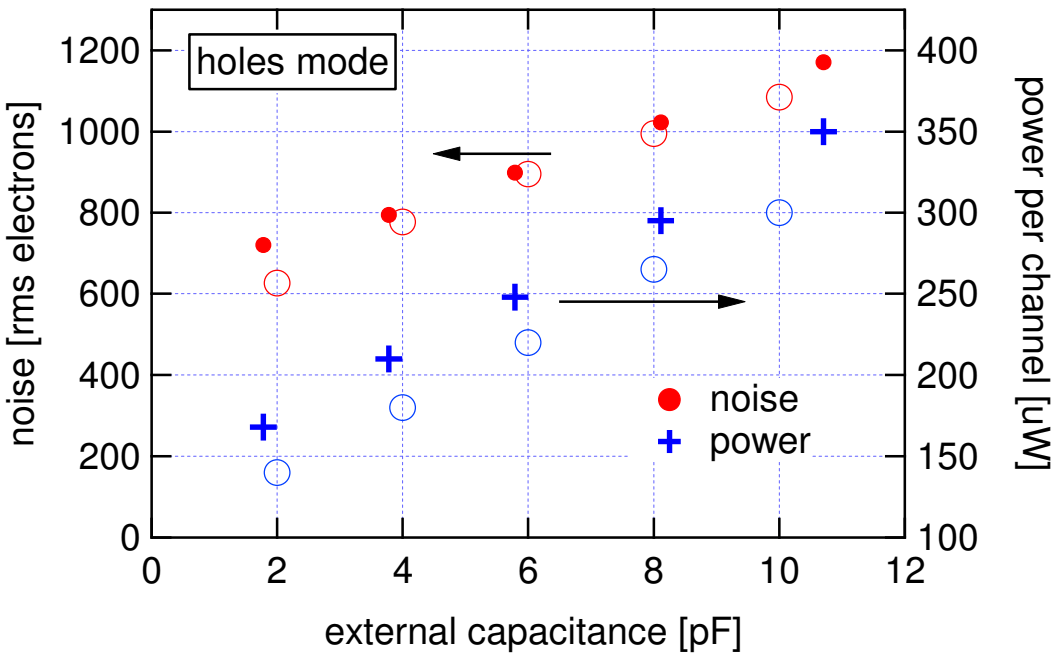
I_{VDDD} = 2.8 – 4.5 mA for whole chip

(depending on SLVS bias setting)

< 50 µW / channel

no measurable dependence on L1 trigger rate

(0 – 100 kHz)



total

180 + (21 x C_{SENSOR}[pF]) uW / channel

e.g. < 300 uW for 5 pF sensor capacitance

(c.f. APV25 ~2.7 mW / chan. (but long strips))

the triggering challenge

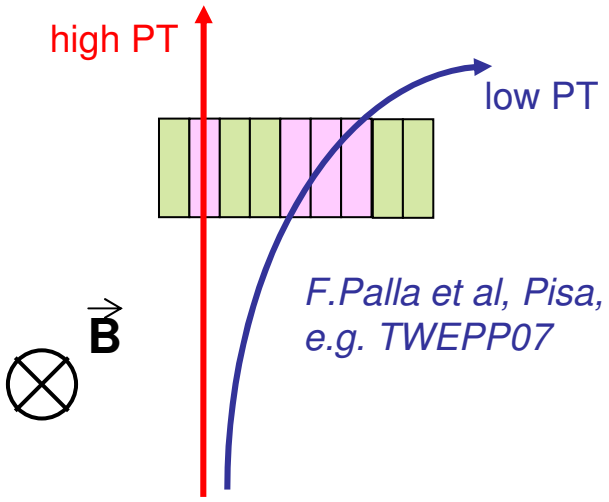
not possible to maintain 100kHz L1 trigger rate
without information from tracker

impossible to transfer all data off-detector
=> on-detector data reduction

2 approaches identified - CWD and stacked tracking
(can be combined)

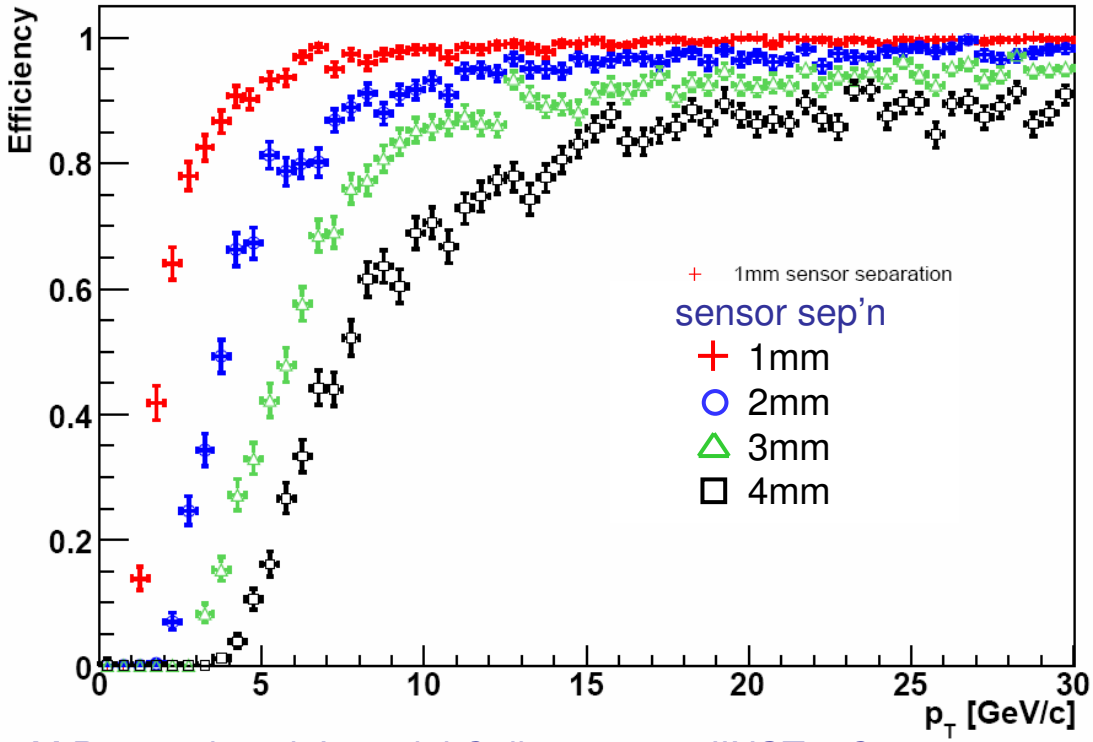
cluster width discrimination

high PT track -> narrow cluster width



F.Palla et al, Pisa, e.g. TWEPP07

stacked tracking efficiency vs. PT

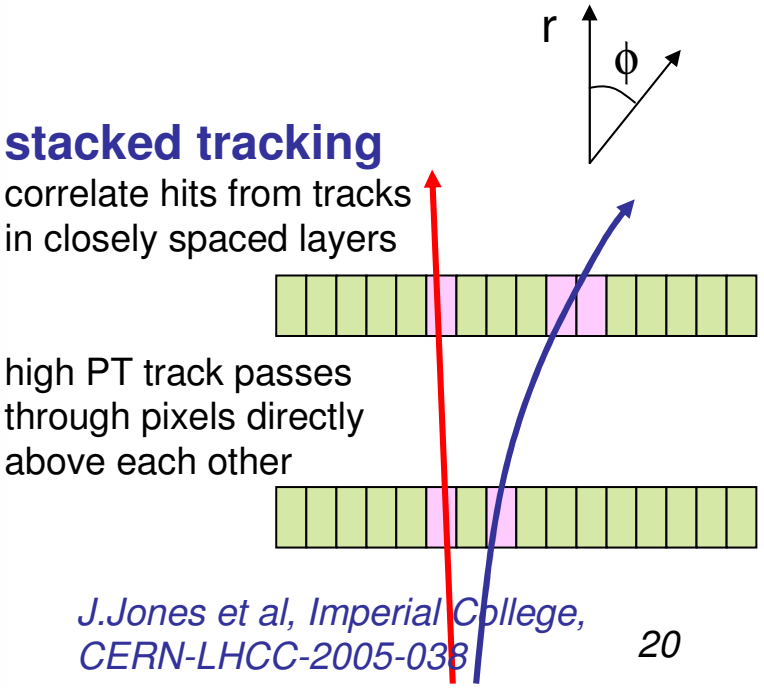


M.Pesaresi et al, Imperial College, 2010 JINST 5 C08003

stacked tracking

correlate hits from tracks
in closely spaced layers

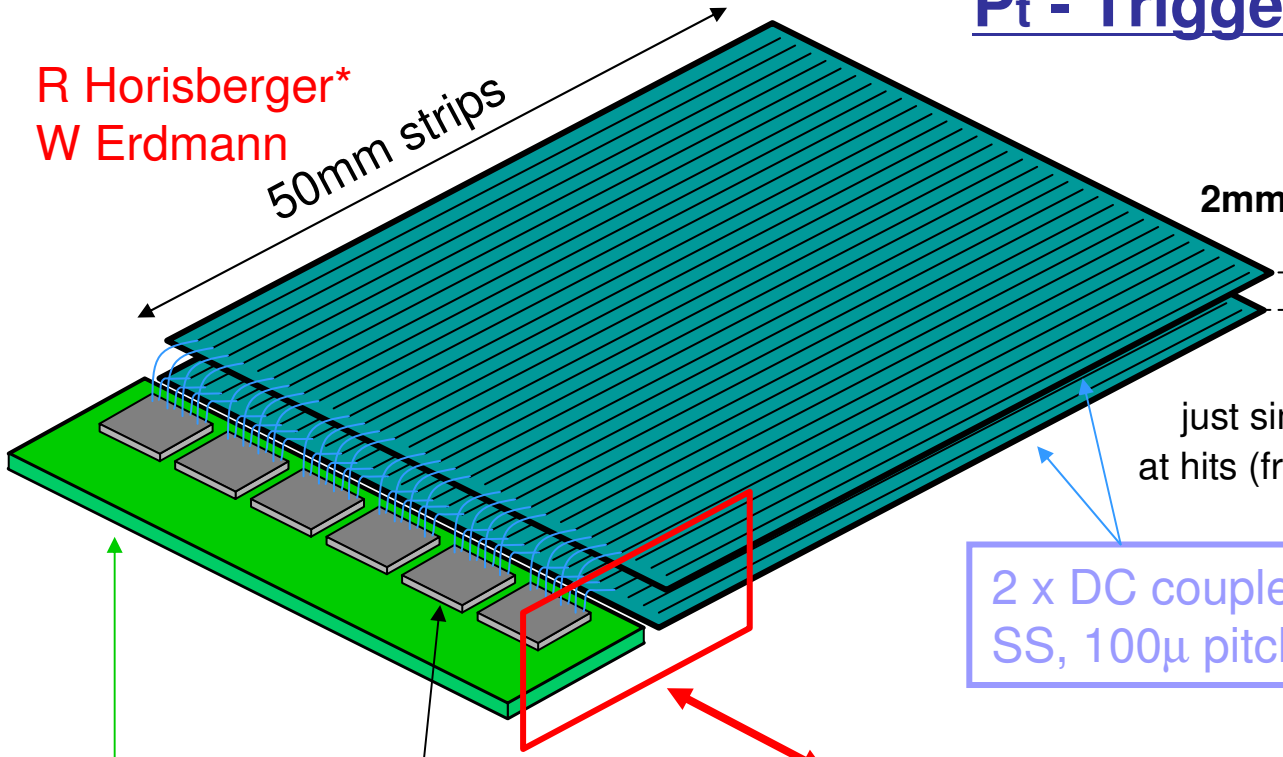
high PT track passes
through pixels directly
above each other



J.Jones et al, Imperial College, CERN-LHCC-2005-038

P_t - Trigger for TOB layers

R Horisberger*
W Erdmann



"Two-In-One" Design

bond stacked upper and lower sensor channels to adjacent channels on same ASIC

no interlayer communication

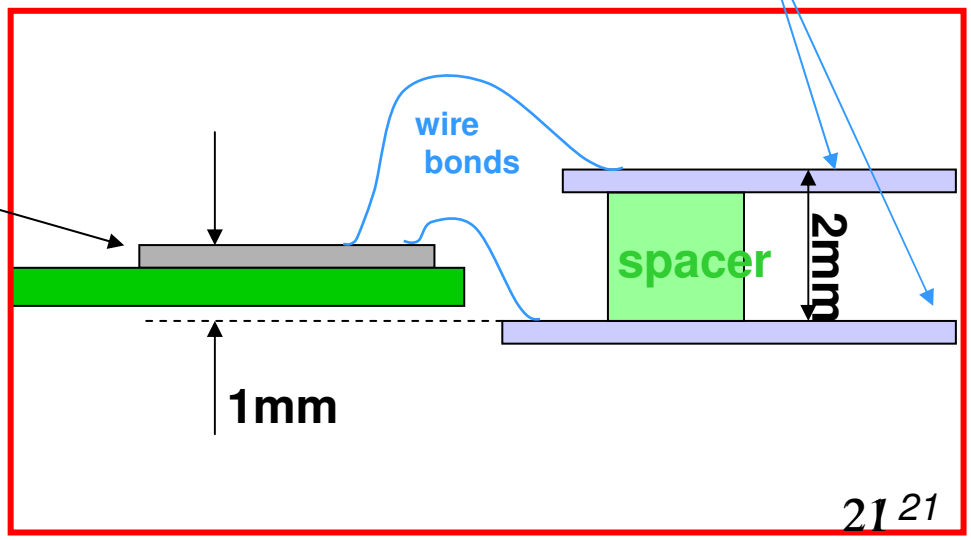
no extra correlation chip

just simple logic on readout chip, looking at hits (from 2 layers) on adjacent channels

2 x DC coupled Strip detectors
SS, 100µ pitch ~8CHF/cm²

Strip Read Out Chip
2 x 100µ pitch with
on-chip correlator

Hybrid

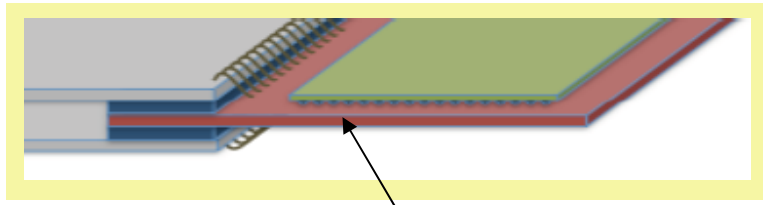


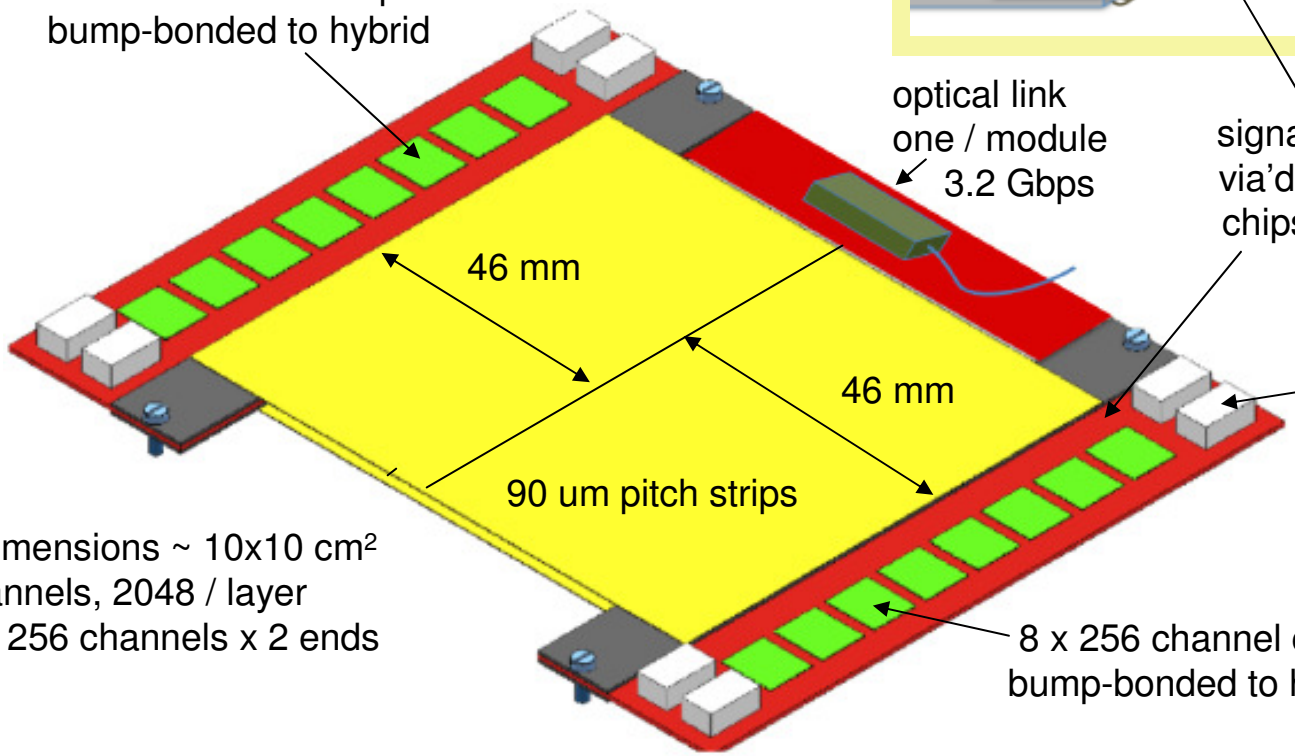
track angular resolution ~20mrad

→ good P_t resolution

* *http://indico.cern.ch/getFile.py/access?contribId=3&sessionId=0&resId=0&materialId=0&confId=36580*

more “hi-tech” 2-in-1 module concept



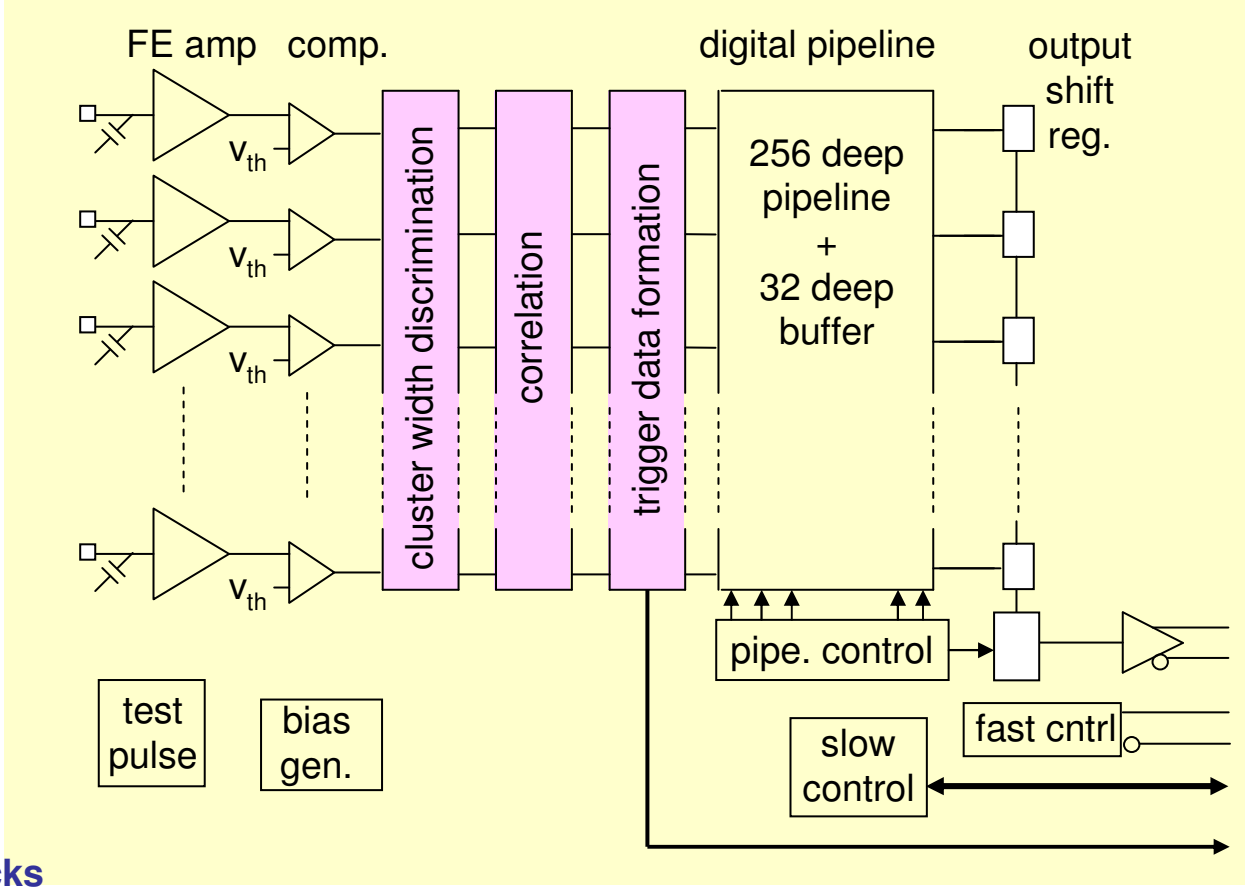


sensor dimensions ~ 10x10 cm^2
4096 channels, 2048 / layer
8 chips x 256 channels x 2 ends

R&D required into

- use of System-in-Package substrate technology - but unconventional size
- optical link package - small dimensions required
- ….

CBC modifications for 2-in-1 concept



3 new blocks

cluster width discrimination

wide clusters within a sensor layer not consistent with high PT track - electronically simple

correlation

do the stacked tracking operation - electronically relatively simple

trigger data formation and off-chip transmission

options under discussion

either synchronous => limited no. of stubs per BX

or asynchronous => no hard limit, but buffering & timestamping required.

SLHC layout picture

modules in red: outer tracker
strip PT modules just described

all ~ 10x10 cm², **including** end-cap
(negligible effects from overlaps)

4 trigger stubs track

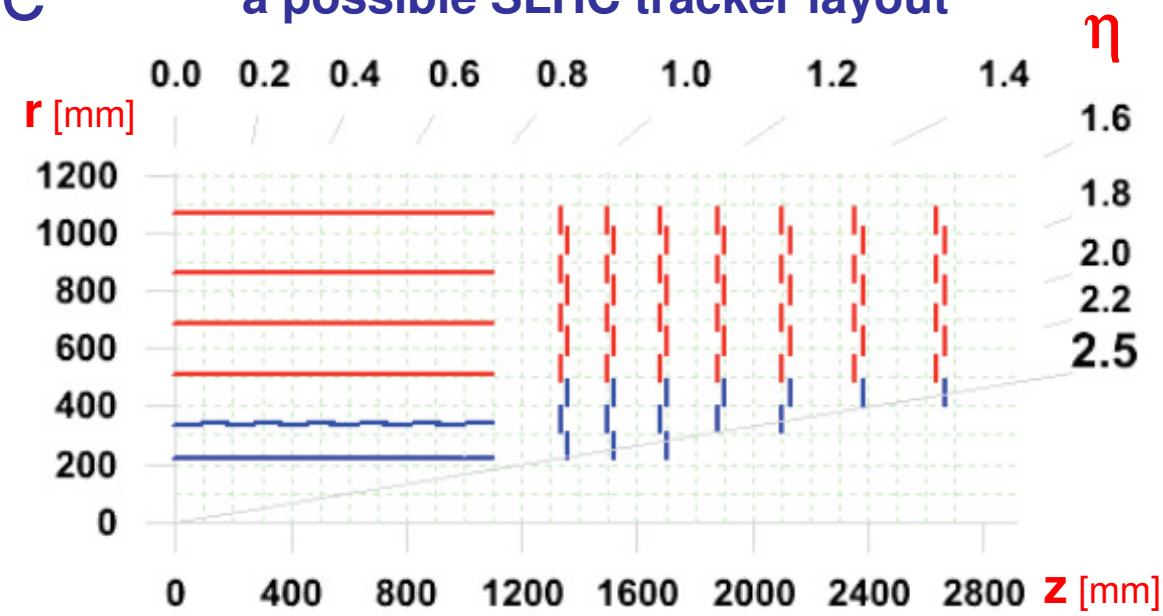
some R&D required but seems feasible

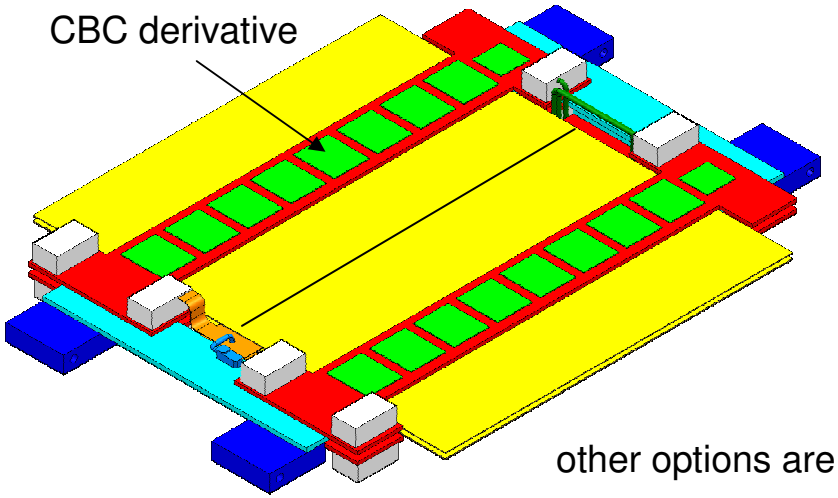
modules in blue:
could be:

short strips ~2.5cm, stereo to give better z res'n, at least for trigger**ed** data

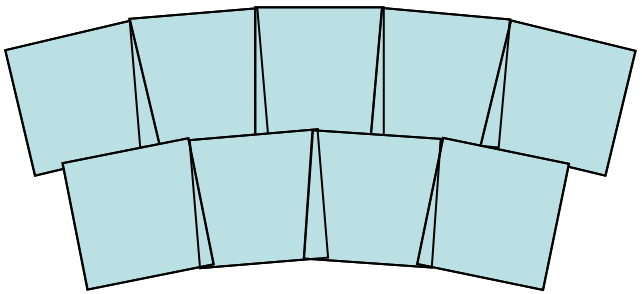
pitch adaption in substrate

a possible SLHC tracker layout





square modules in end caps



other options are under consideration

summary

LHC

strip tracker readout based on 0.25 μm APV performing well

APV has also proved popular elsewhere

COMPASS (~2,500), BELLE (~5,000), STAR(~3000), HADES, NASA, NA47, RD51, OLYMPUS, PANDA, ZEUS, ..
mainly silicon and GEM readout: analogue, unsparsified info attractive

SLHC challenges

power

consumption: technology can help, but number of channels increases
delivery: CMS plan to us DC-DC conversion on front end

triggering

module concepts using cluster width discrimination and stacked tracking approach seem promising

CBC

130 nm prototype for short strip readout working quite well

already providing valuable information

e.g. performance achievable and power budget required

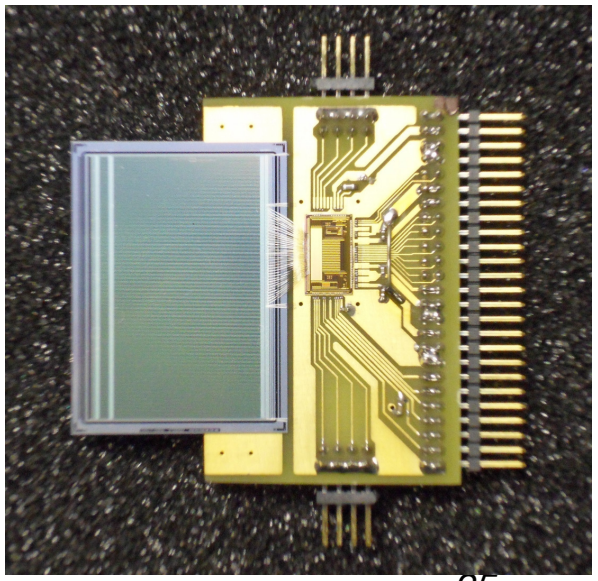
long testing programme ahead, including

powering options, temperature effects, tests with sensors
radiation: ionizing & SEU sensitivity, test beam

next chip iteration

looking at bump-bondable version with triggering features

CBC + sensor



links

CMS Tracker Upgrade web-page:
http://cms-tracker.web.cern.ch/cms-tracker/TKSLHC/index.html

CBC documentation:
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/

extra

alternative module for inner barrel

more recent ideas for inner barrel and end cap rings (blue modules)

a new flavour of PT module - mixed strips and pixels

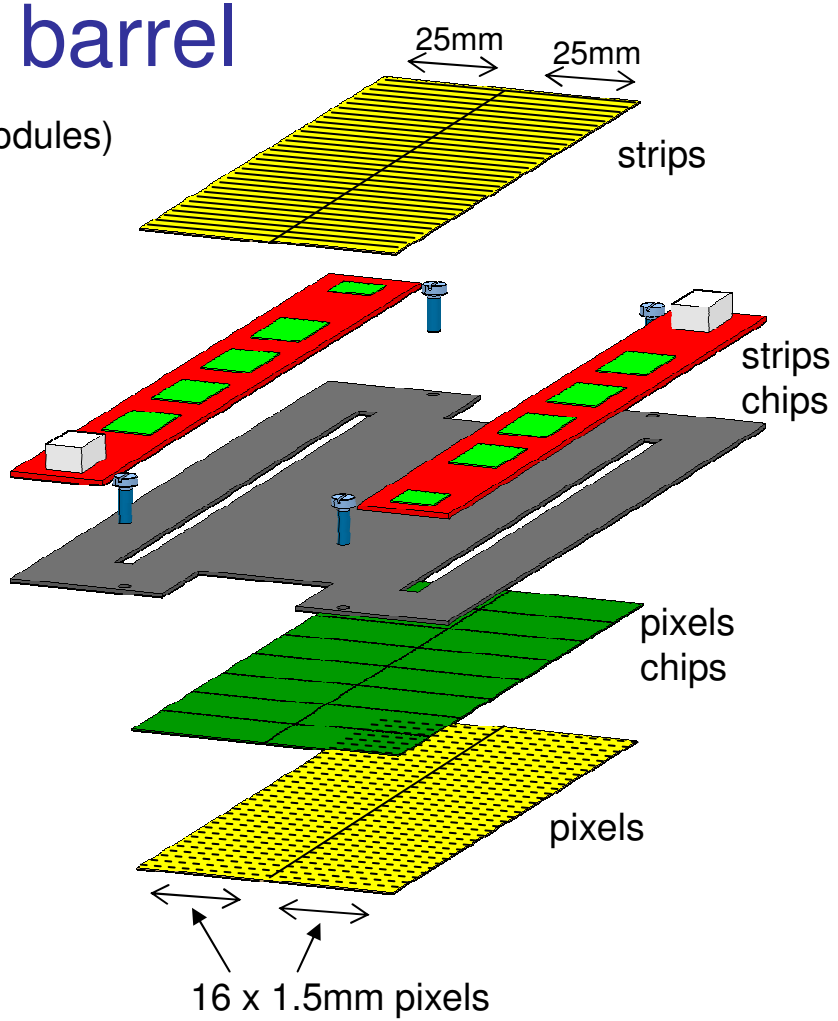
one layer of strips ~ 25 mm long (1/2 module)
one layer of pixels 25/16 = ~1.5 mm

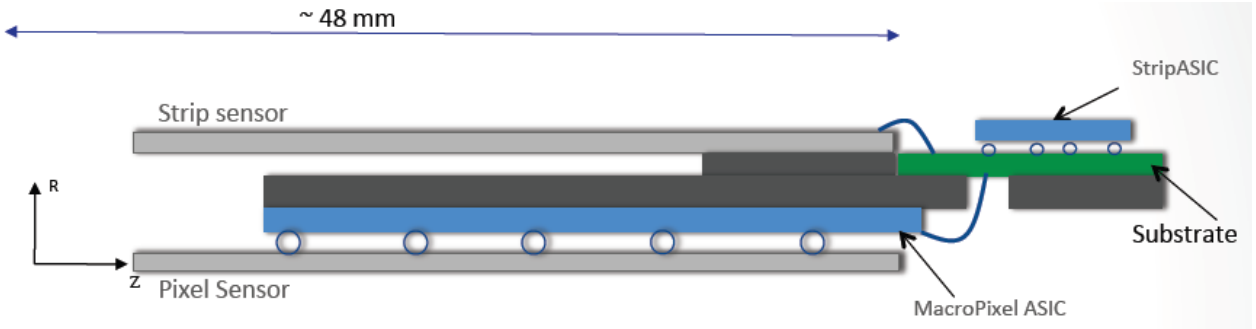
pixels ORed in z direction
effectively making a single strip in z direction

perform correlation with strips layer

resulting stubs transmitted, **but** including pixel address

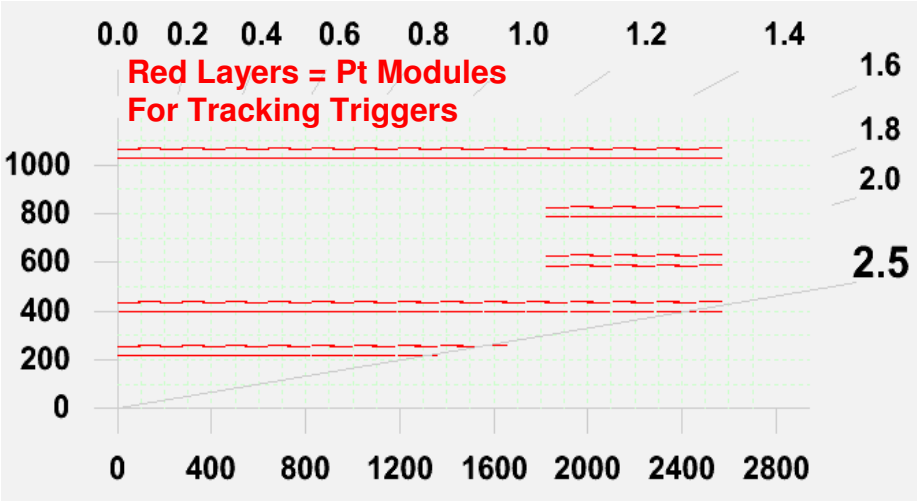
more challenging
module and layer design, data volume, power,…

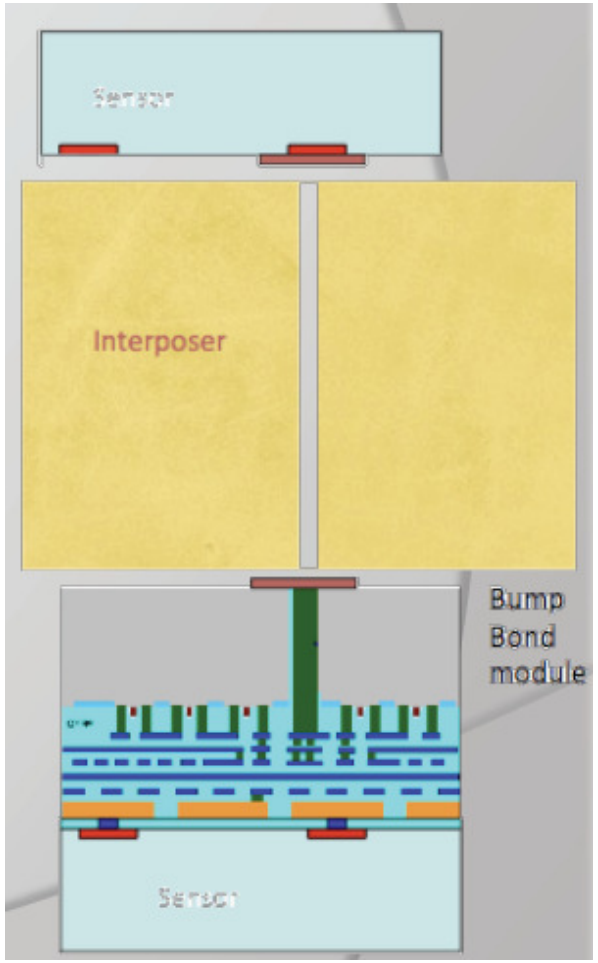




long barrels option

e.g. see R.Lipton
https://indico.cern.ch/getFile.py/access?contribId=9&sessionId=12&resId=1&materialId=slides&confId=136197





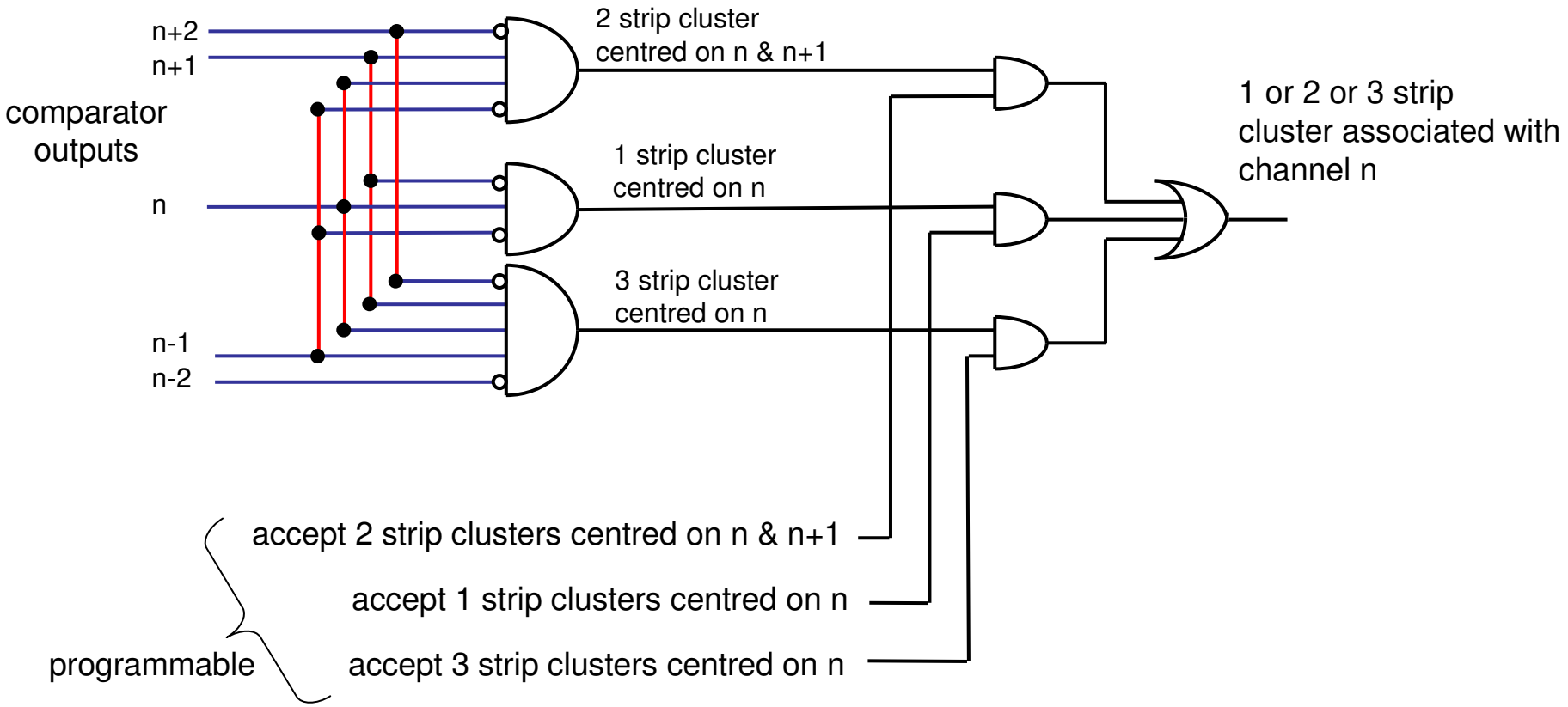
3D electronics

single chip connects to top and bottom sensors
analogue paths through interposer from top strip sensor
bottom sensor ~mm pixels

electronics and connectivity technologically challenging

under prototyping, but a long way to go for large surface and volume production

cluster width discrimination



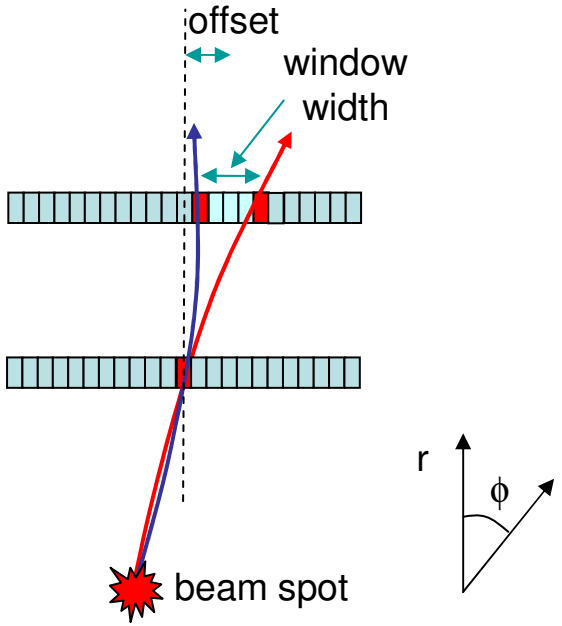
n-1, n, n+1, … are neighbouring channels on one sensor layer (inner or outer)
(but every other channel on chip)
could increase to accept wider clusters if necessary

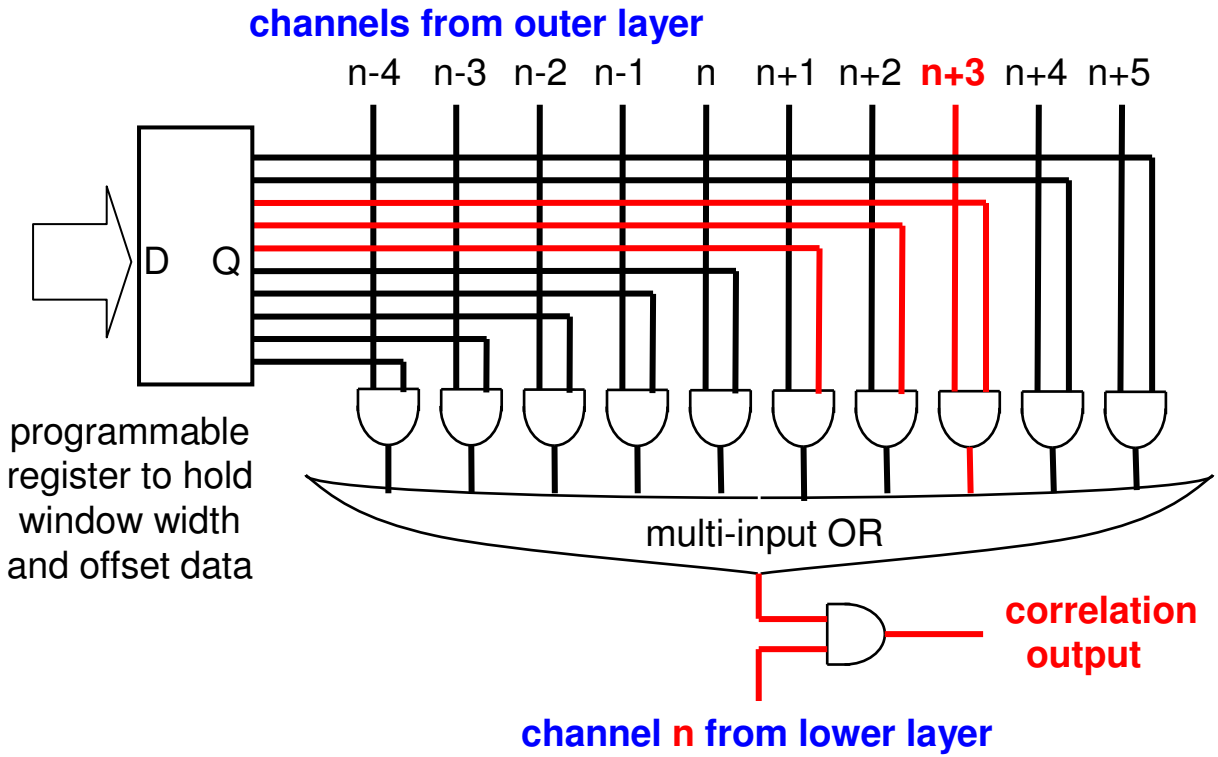
correlation and offset correction

want to correlate cluster in lower layer with cluster occurring within window in upper layer

need programmability of cluster window width
width depends on P_T threshold cut
(narrower window => higher P_T threshold)

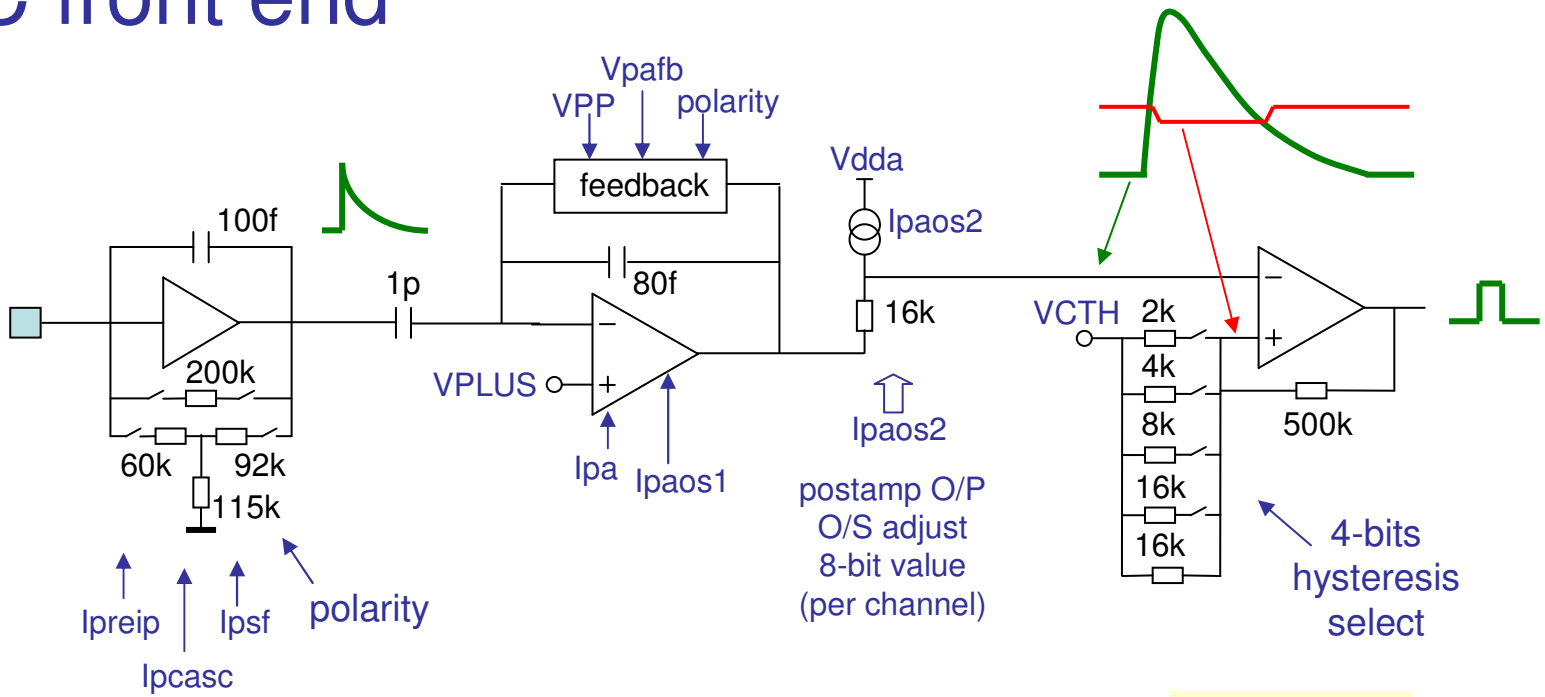
lateral offset of window centre will vary across module





need one of these circuits on every channel
programmable register inputs to AND gates to allow for cluster window and offsets between layers
offset varies depending on location across sensor
in above example 2 channel offset applied to 3 channel window in outer layer
cluster on channel **n+3** in outer layer correlates with cluster on
channel **n** in inner layer

CBC front end



preamp
resistive feedback absorbs I_{leak}
T network for holes
Rf.Cf implements short diff. time constant
(good for no pile-up)

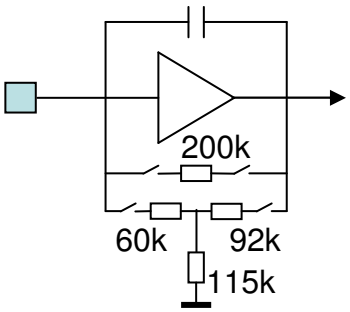
postamp
provides gain and int. time constant
~ 50 mV / fC
AC coupled removes I_{leak} DC shift
individually programmable O/P DC level
implements channel threshold tuning
8-bits, 0.8 mV / bit, 200 mV range

comparator
global threshold
(indiv. tuning at postamp O/P)
programmable hysteresis

leakage current tolerance

Ileak absorbed by preamp
resistive feeback

=> DC shift at preamp O/P



electrons mode

single 200k resistor, leakage shifts output +ve

plenty of headroom

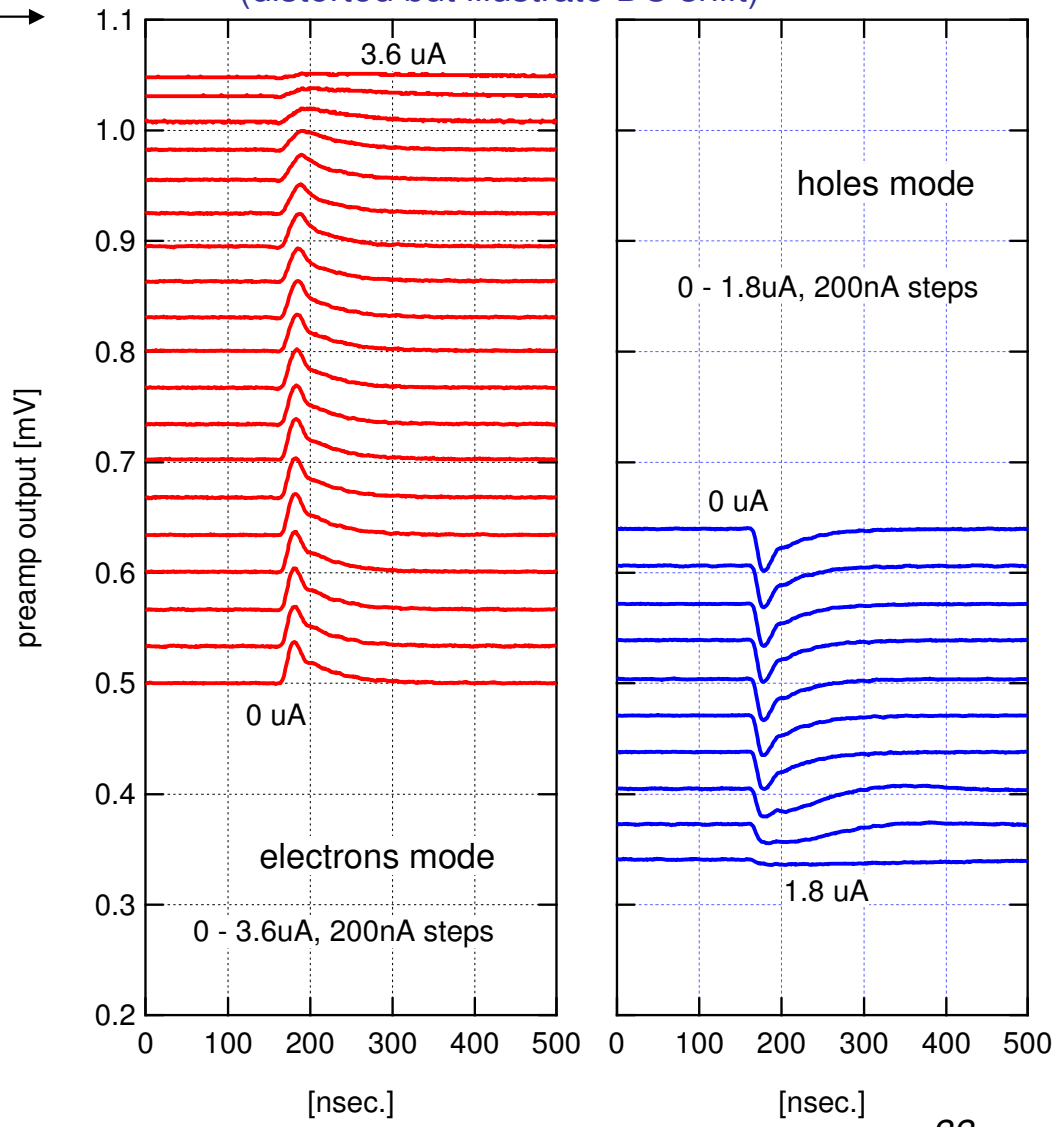
holes mode

T network produces +ve offset
leakage shifts output -ve

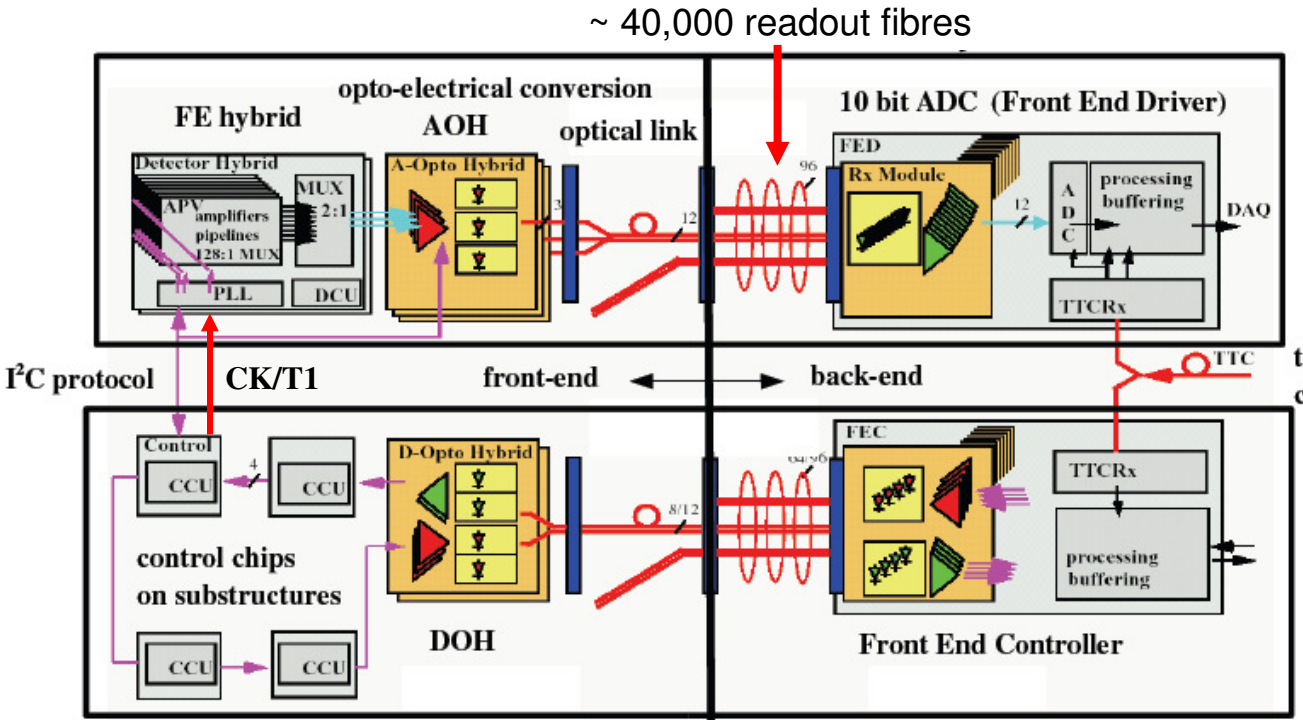
sufficient headroom for 1 uA

(note: waveforms include ~ 300 mV offset
due to source follower on test channel O/P)

waveforms measured on test channel
(distorted but illustrate DC shift)



control system



digital optical control link
from FEC -> front end provides
Ck/T1 and control data

opto-electrical conversion
on front end

CCU chip electrical control ring
architecture on front end reduces
no.of control fibres required

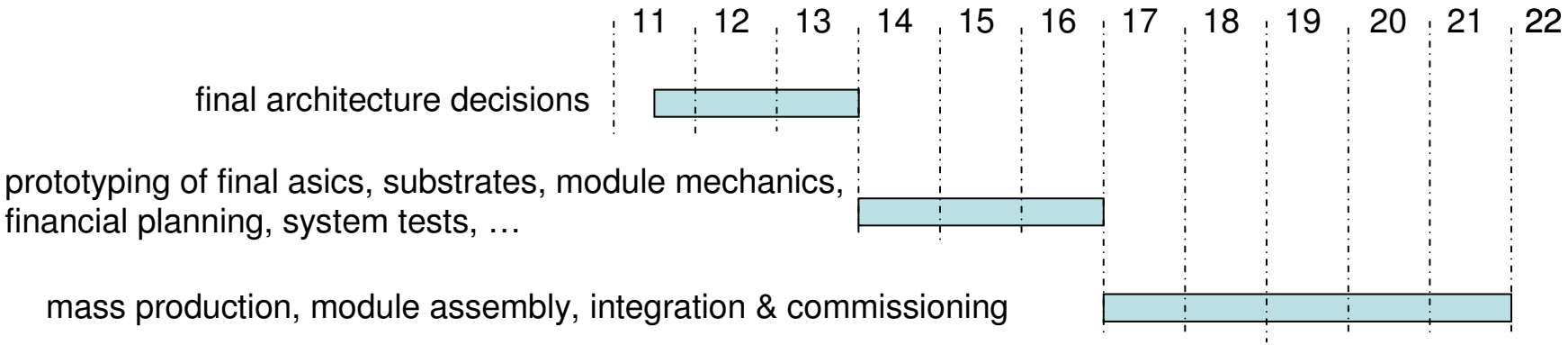
each CCU provides
Ck/T1 and I²C control buses
to up to 16 FE modules

I²C used for:

- programming APV registers (bias generation and operation mode)
- reading DCU monitoring info (voltages, currents, temperatures)
- setting up optical link system (laser driver gain, bias currents)

Phase II schedule

my thoughts



not long left before final decisions on architectures
Technical Design Report ~ 2013?