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Silicon Detectors R&D future needs and opportunities for European collaboration

Joost Vossebeld

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Performance requirements future experiments

Technology Driver / Target Application	Pixel Size (Granularity)	Pixel Size (Resolution)	Radiation Hardness	Timing Resolution	Radiation Length	Collection Thinness	Cost per Area	Low Power
HL-LHC Vertex								
HL-LHC & LHCb Tracker upgrades								
LHCb Phase 3 Vertex								
Future hh Vertex								
Future hh Tracker								
Future hh HG ECAL								
Proton EDM								
Future e-h								
Nuclear Physics incl. HI & FAIR								
e^+e^- Vertex (ILC/circular)								
e^+e^- Vertex (CLIC)								
e+e- Tracker (ILC/circular)								
e^+e^- Tracker (CLIC)								
e^+e^- HG ECAL								
cLVF rare muon decays (Mu3e)								
Hadron Therapy								

Matrix identifying R&D priorities for different experiment areas

Pixel size (granularity) & Radiation hardness → HL-LHC, FCC-hh and other high rate experiments

Timing resolution → tracking in high density environment

Pixel size (resolution) → Future e^+e^-, other precision experiments

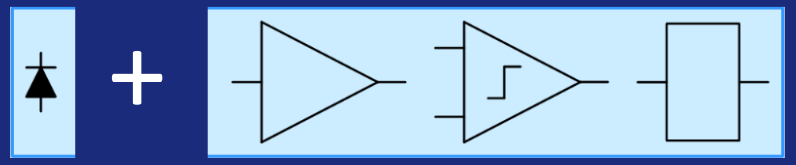
Collection thickness → HG calorimetry (MIP counting)

Large area (cost) → HG calorimetry and tracking at collider experiments

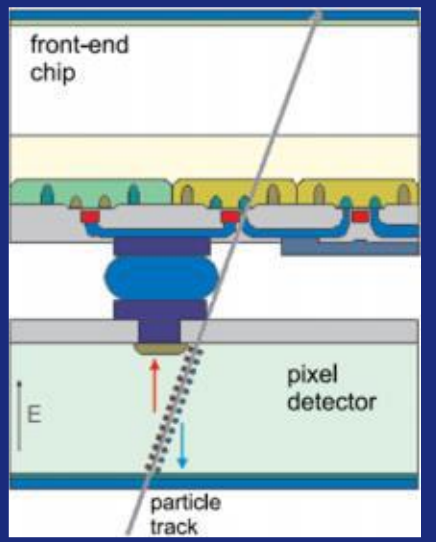
Low power & Radiation length → all

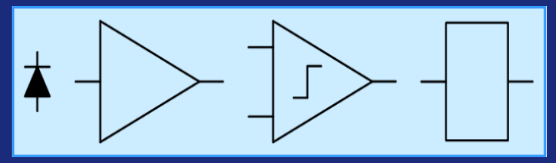
Adapted from document submitted as input to PPAP strategy review in 2017:
https://conference.ippp.dur.ac.uk/event/542/contributions/3021/attachments/2568/2808/Statement_to_PPAP_on_CMOS_RD.pdf

MAPS vs Hybrid sensors

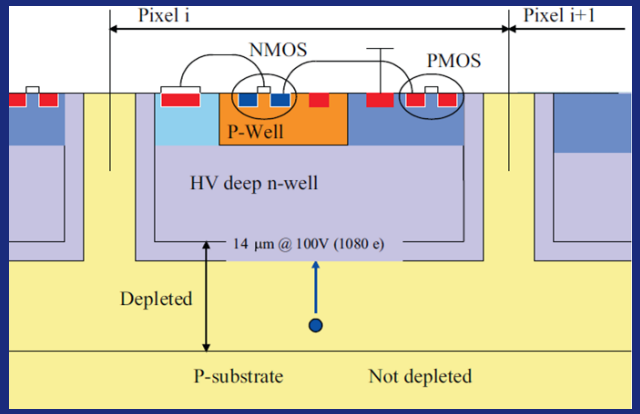


Hybrid sensors:
Sensors diode and electronics on separate wafers.
Most common choice in today's strip and pixel detectors.
Typically custom high purity planar silicon sensor bump or wire bonded to a CMOS read-out ASIC.

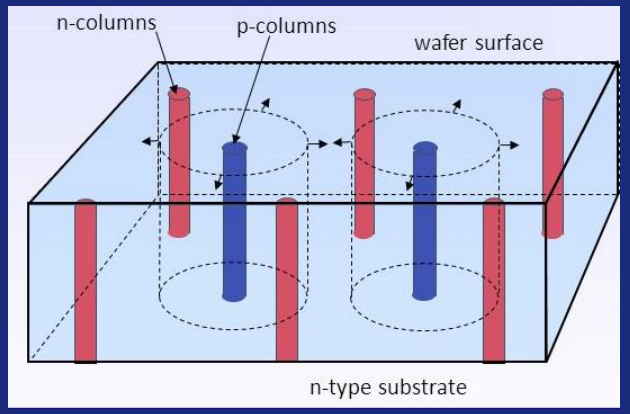




Monolithic active pixel sensors (MAPS)
Sensors diode and electronics on the same wafer in CMOS technology. Variations as to how much for the logic is in the pixel or the periphery.



Hybrid sensors



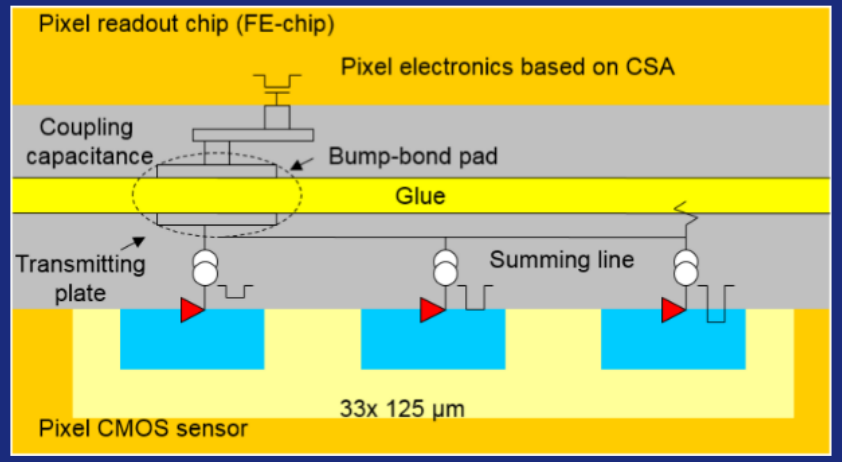
Planar silicon sensor bump or wire bonded to a CMOS read-out ASIC.

Major advantage is ability to use custom technology and diode layout of the sensor.

Established technology used for tracking/vertexing in most PP experiments

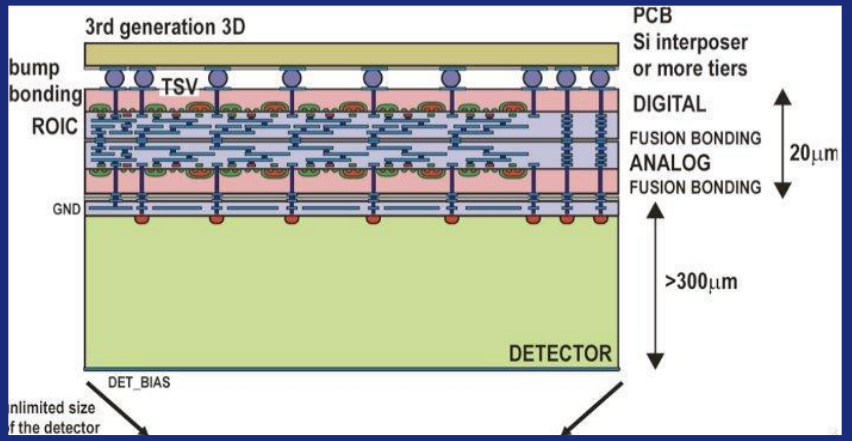
Current state of the art (n-in-p or 3D-columns) in radiation hardness, ~10^{16} neq.

Disadvantages (for pixels) are complex and high costs for assembly, higher mass and the need for bump-bonding, which limits the minimum pixel size.



Active areas of R&D Developments

- Push radiation hardness through modifications to process and diode layout, in-sensor charge amplification.
- Remove need for bump-bonding using ***capacitive coupling (CCPD)***
- 3D interconnection technologies: small pitch bonding, through-silicon-vias, etc
- Full 3D integration (wafer stacking). High level of integration of analogue and digital electronics, whilst keeping signal path very short (low noise) and the overall device very thin



Hybrid sensors provide route to meeting the most extreme performance requirements. Due to cost they are less attractive for pixel tracking requiring large area coverage.

Sensors with integrated electronics CMOS-MAPS, CCDs, DEPFETs, ..

Long standing R&D for future e^+e^- collider.

Used in heavy flavour (DEPFETs in Belle), heavy ion physics (CMOS-MAPS in STAR and ALICE).

Shallow collection depth means sensors can be very thin (~50µm).

Belle II DEPFET sensor

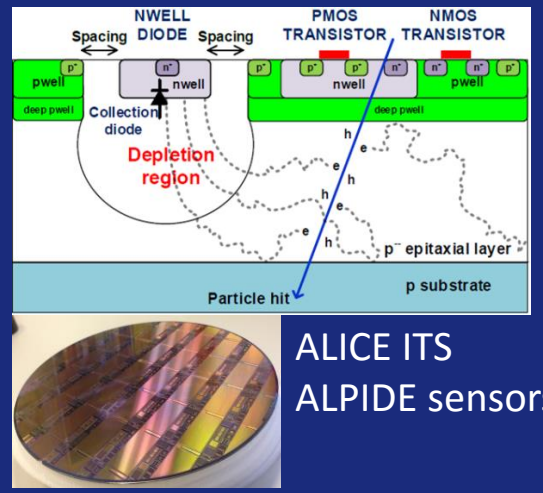
Most R&D probably going on CMOS-MAPS

- Industry standard technology (p/n-mos transistors, small feature size, multiple metal layers)
- Ease of assembly
- Cost effective production (thinning or other custom processes can drive the price up again).

Best position resolution 1-2 µm

- MAPS, CCD and DEPFETs can have very small pixels.
- Further improvement resolution through charge sharing.

Limited perfomance on radiation tolerance ($2x10^{13}$ neq/cm^2) and readout speed: ~100 ns



ALICE ITS ALPIDE sensors

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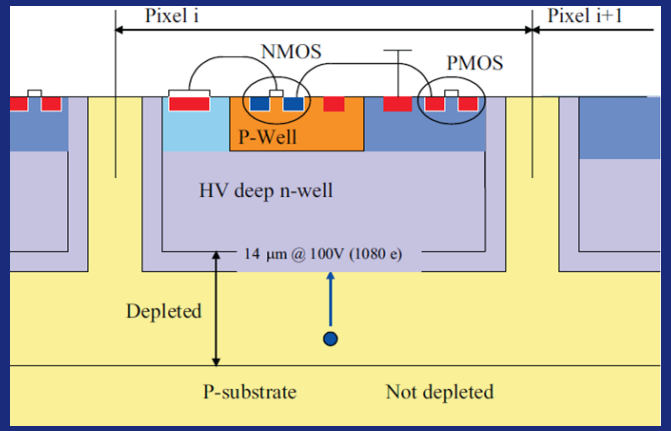
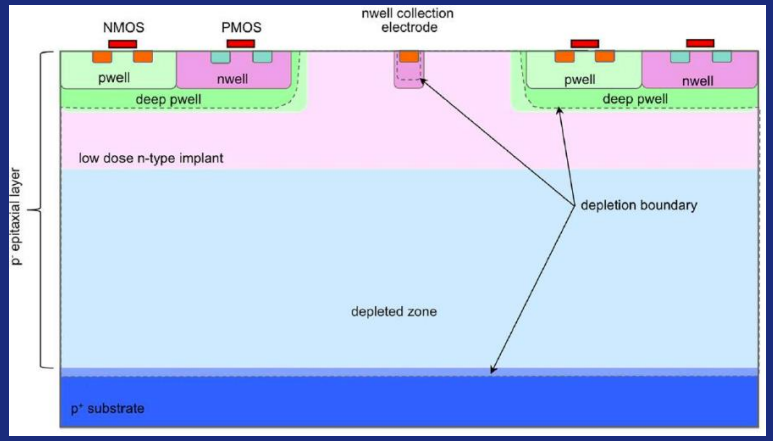
Depleted-MAPS

In standard CMOS charge is collected by diffusion. If the sensor bulk can be depleted the induced E-field will result in charge collection by drift. (High-Voltage-CMOS or High-Resistivity-CMOS)

Higher signal and faster charge collection. This allows to combine the benefits from Hybrid sensors (radiation tolerance and speed) with those of MAPS (integration of analogue and digital logic, lower cost,lower material).



I. Peric,
NIMA 650 pp. 158-162, 2011

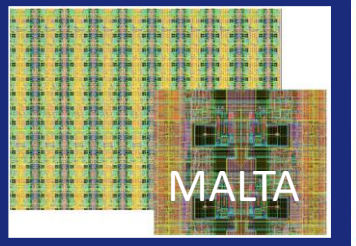


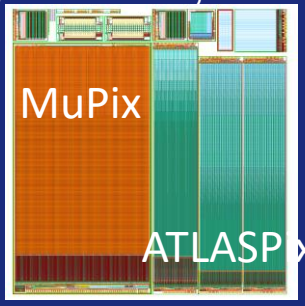
W. Snoeys et al.
DOI 10.1016/j.nima.2017.07.046

Achievements to date: pixel sizes 50x50 µm^2 ; radiation tolerance to ~2x10^{15} neq/cm^2; timing 10-15 ns ; shallow collection depth allows thinning to 50 µm.

Active R&D:

- Sensor development for Mu3e and ATLAS HL-LHC pixels
- Generic R&D to push down timing resolution <1 ns (RD50)





Timing resolution for 4D tracking and vertexing

In high occupancy experiments accurate timing information can help to reject hits or tracks from pile-up.

What is needed? At LHC need <100ps to discriminate between tracks from different vertices in a single bunch crossing.

- Track to vertex association with **a single timing layer** to reject tracks from pile-up vertices
- Timing measurement **in all layers** would also reduce the combinatorics in track finding.

  Need to keep small pixels for position resolution

Current performance:

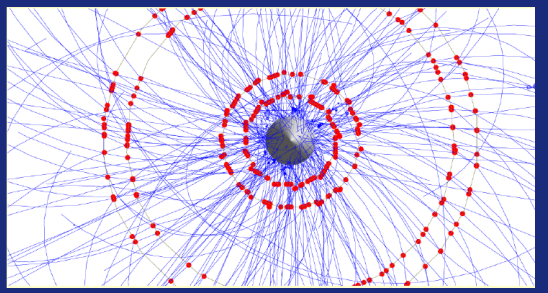
- 30-35 ps in sensors with gain (LGAD, SiPM), but sensing elements are typically a few mm^2
- In hybrid or depleted CMOS (small pixel) devices 10-20 ns is routinely achieved, O(1 ns)

  should be feasible

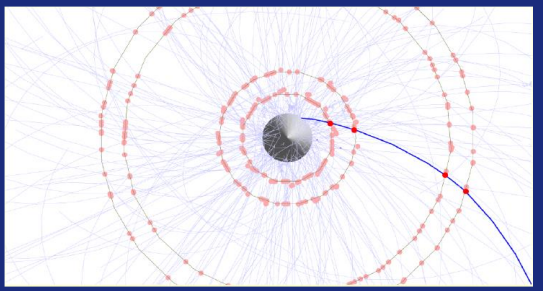
Future R&D:

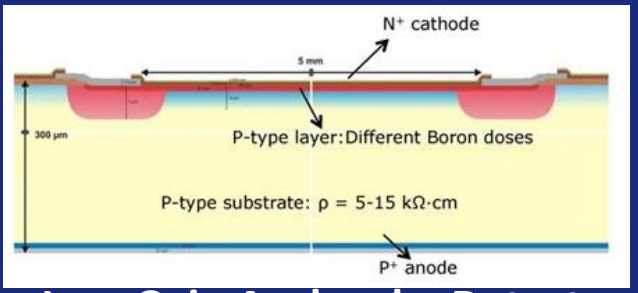
- difficult to go much below 30 ps in a single measurement (due to fluctuations in deposited charge). Use stacking to incorporate multiple measurements in a single wafer?
- push for sub ns timing in small CMOS pixels, very small feature sizes in HV-CMOS may achieve charge amplification.

Mu3e 10^9 μ/s with 50 ns frame



Mu3e 10^9 μ/s with 1 ns frame





Low Gain Avalanche Detector

G. Pellegrini et al., NIMA765 (2014) 12

Closely related R&D

In addition to R&D on sensor technology there is also a broad effort pursuing related technology aspects, (much of this strongly supported through AIDA & AIDA2020!)

Readout ASICs and front-end electronics

Interconnect technologies:

- Small pitch solder bump bonding to allow for smaller pixel hybrid sensors
- Capacitive coupling (through a very thin glue layer)
- Through Silicon Vias and wafer-to-wafer bonding for simplification of assembly or 3D stacking

Low mass mechanics:

- Support structures
- Air cooling,
- Micro-channel cooling
- Curved silicon sensors

Improved ease of tiling through larger detectors and lareg sensitive area

- Stitching to achieve larger area pixel sensors (beyond the typical mask reticule size of 2x2 cm^2 or 2x3 cm^2.
- Development active edge technology

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What should the European Strategy Update say on Silicon R&D?

Successful R&D needs requires sustained effort and resource.

The effort should:

- push the performance of applications in new/existing technologies
- adopt promising technology improvements developed outside
- work on more fundamental technology R&D for the longer future

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The 2013 European Strategy Update on R&D

IMPORTANCE OF DETECTOR R&D FOR PP: "The success of particle physics experiments, such as those required for the high-luminosity LHC, relies on innovative instrumentation, state-of-the-art infrastructures and large-scale data-intensive computing. Detector R&D programs should be supported strongly at CERN, national institutes, laboratories and universities. Infrastructure and engineering capabilities for the R&D program and construction of large detectors, as well as infrastructures for data analysis, data preservation and distributed data-intensive computing should be maintained and further developed."

IMPORTANT AREA FOR KNOWLEDGE EXCHANGE: "Knowledge and technology developed for particle physics research have made a lasting impact on society. These technologies are also being advanced by others leading to mutual benefits. Knowledge and technology transfer is strongly promoted in most countries. The HEPTech network has been created to coordinate and promote this activity, and to provide benefit to the European industries. HEPTech should pursue and amplify its efforts and continue reporting regularly to the Council."

IMPORTANCE OF EDUCATION AND TRAINING: "Particle physics research requires a wide range of skills and knowledge. Many young physicists, engineers and teachers are trained at CERN, in national laboratories and universities. They subsequently transfer their expertize to society and industry. Education and training in key technologies are also crucial for the needs of the field. CERN, together with national funding agencies, institutes, laboratories and universities, should continue supporting and further develop coordinated programs for education and training."

Areas of European cooperation: Access to Industry

Silicon sensor development requires access to a range of commercial technologies:

1. **Software** for integrated circuit design and simulation and associated training
2. **Access to foundries**
3. Custom **wafer processing**: implantation, metallisation
4. Wafer **dicing and thinning**
5. **Interconnection techniques**: solder bump deposition, flip-chip bonding,

An important European project is **EuroPractice**: liaison industry and academia providing access to advanced software for academic users (sensor design and simulation, FPGA programming, ..) access to commercial technologies for R&D submissions and offering a broad training programmes

Currently no common provision for access to 3,4,5. (Challenging for small scale R&D)

Areas of European cooperation: common facilities and tools

Assembly and lab testing: Wire bonding, Wafer probing, lab facilities, readout electronics and firmware. Although not every institute can provide all, these can usually be accessed by inter-institute collaborations

Irradiation facilities with neutrons, protons, other particles. In general we benefit from existing facilities (reactors, irradiation facilities for medical radio isotopes). Access often through associated PP groups that are themselves active in Silicon R&D, through RD50 or informal agreements. Operation costs supported by AIDA2020.

Beam test campaigns. Access to beam – typically at the major labs; Access to beam telescopes - typically available for test beam campaigns (supported AIDA, AIDA2020)

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For discussion: possible further recommendations for the strategy review

- A strong message that the physics reach of PP experiment is and remain closely linked with progress in detector R&D
- Affordable access to design software, provided by EuroPractice, is critical and should be maintained.
- Detector R&D, in particular for Silicon is expensive. The provision of common infrastructure and tools for example for small batch bump-bonding, dicing, thinning, other processing, could enhance lower the threshold for and speed up R&D.
- Similarly, the development of common libraries (similar to open source software) for design blocks in different technologies could provide a substantial boost to development work.
- Access to beam test facilities as well as irradiation facilities is critical to sensor developments and should be maintained.
- CERN RD50 and RD53 collaborations provide a long term platform (beyond the lifetime of single detector projects) and have been important drivers of progress in their respective fields. These should continue to be supported.
- Keep open mind on scope for more RDXX collaborations in R&D areas that require particularly high resource. E.g. CMOS sensors, development of TSVs and wafer-to-wafer bonding.

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BACK-UP SLIDES

Existing International programmes

What cross-European (or wider) coordination is already in place?

- **EuroPractice**: platform for training, distribution of software licenses for academic use (sensor design and simulation, FPGA programming, ..) access to foundries for R&D submissions
- **AIDA & AIDA2020**: broad PP technology development project, including work packages on: interconnect technologies, provision of irradiation facilities, low mass mechanics and cooling solutions, large area cost effective sensors

Sensor programmes (in Europe)

- **CMOS MAPS** sensor programme (ILC, STAR, ALICE ITK) also linked to development x-ray and photosensors
- **Depleted MAPS** (HV-CMOS, or modified technology ALICE chip) for HL-LHC (so far mostly ATLAS), Mu3e, ..
- **Timepix** programme (Fast small pixel sensors) (LHCb VELO upgrade,..)
- **RD50**: generic R&D on radiation tolerance in planar, 3D, HV-CMOS,..)
- **RD53**: ASIC development in 65 nm technology