Status of CALICE ECal

the CALICE ECal Group

CALICE - Electromagnetic Calorimeter

- A tungsten/silicon sampling calorimeter

- Design well advanced, first stack produced

- Silicon wafers in production – high quality verified

- Readout PCB designed – production set

- Very front-end readout chips produced

- Single Slab DAQ system developed for first full chain readout and channel calibration

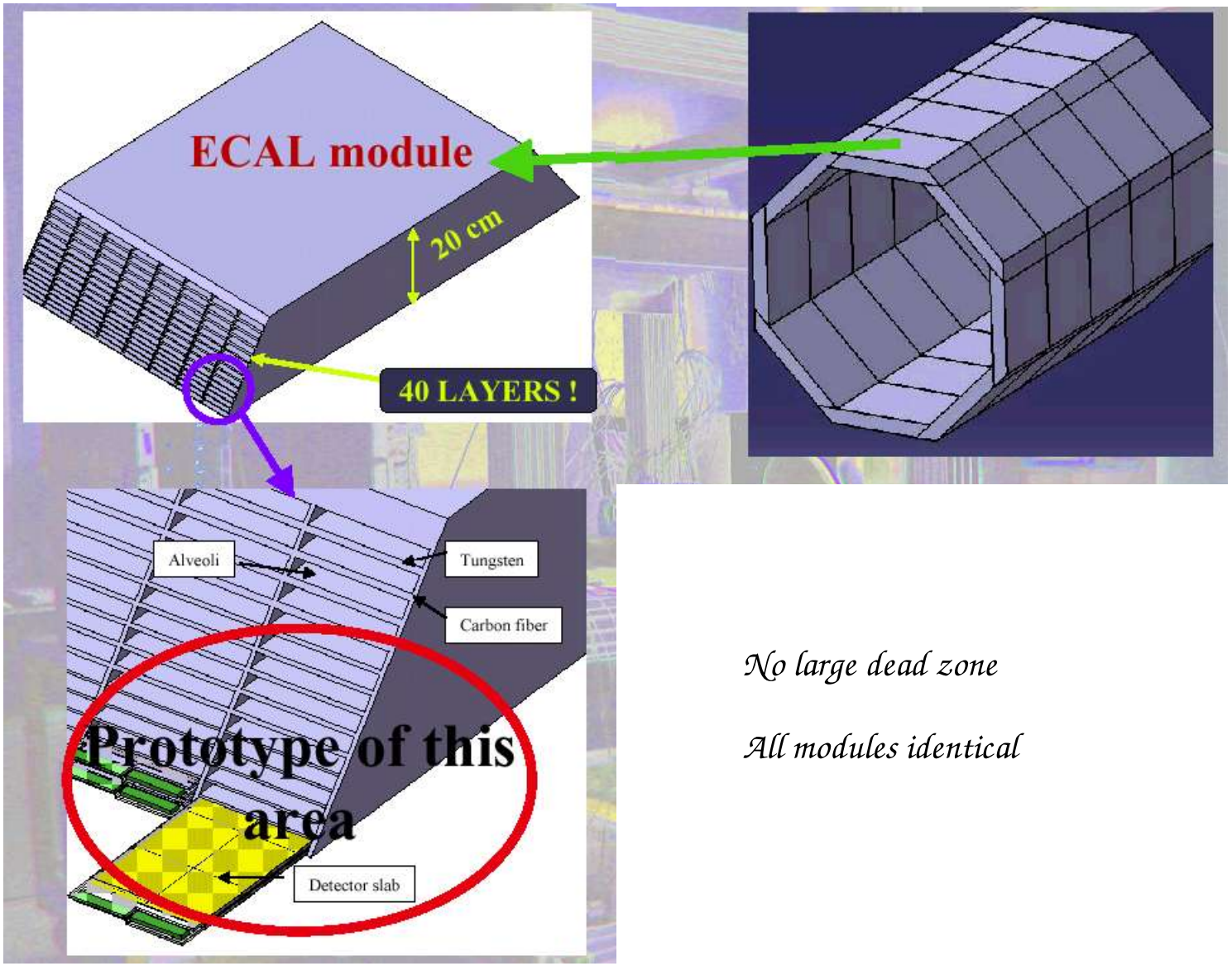
- VME DAQ system for full prototype being developed

⇒ Very active program towards test beam

– end of 2004 (low energy electrons)

- 2005-6… hadrons and electrons

ECal System Design



No large dead zone

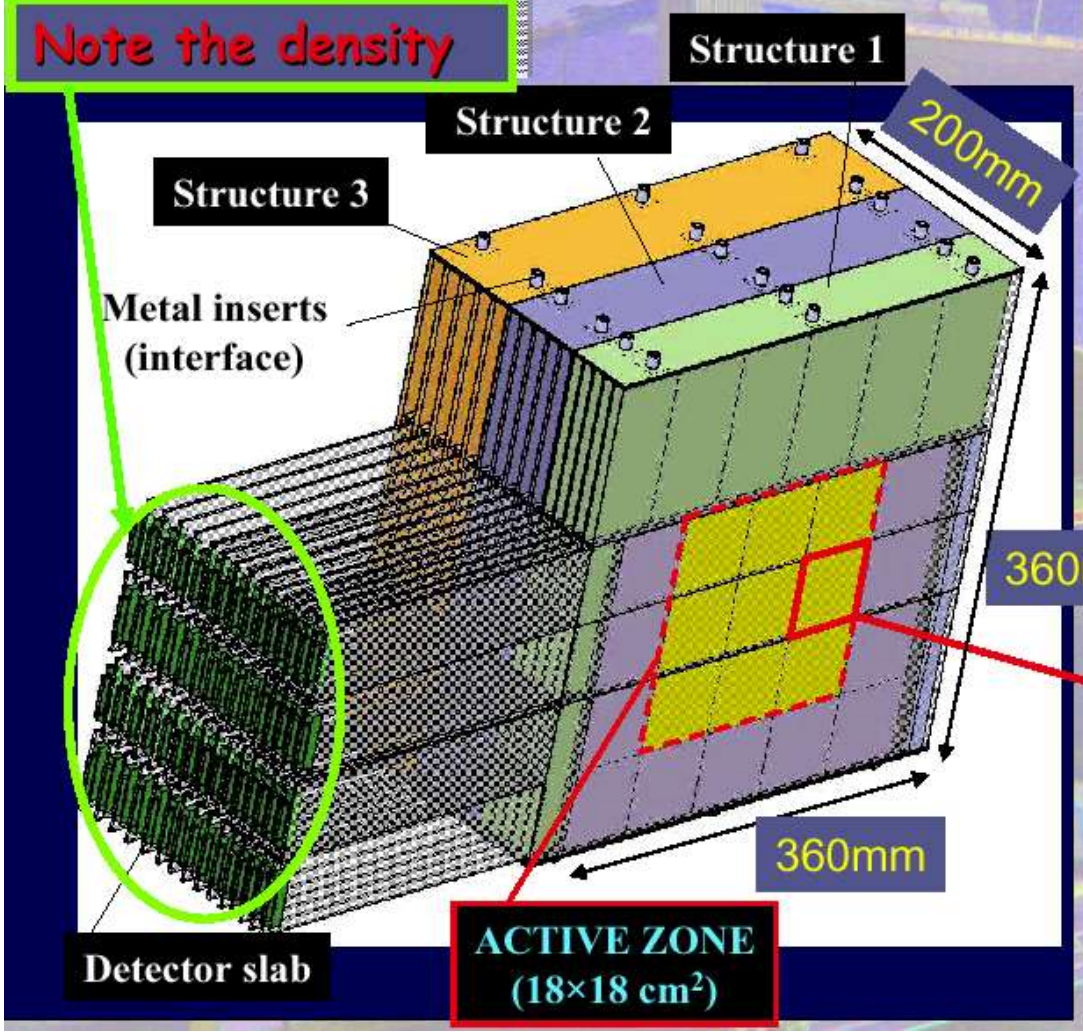
All modules identical

The ECAL prototype

CALICE ECAL

- LAL,LLR,LPC,PICM
- Imperial College, UCL, Cambridge, Birmingham, Manchester, RAL
- ITEP,IHEP,MSU
- Prague (IOP-ASCR)
- SNU,KNU

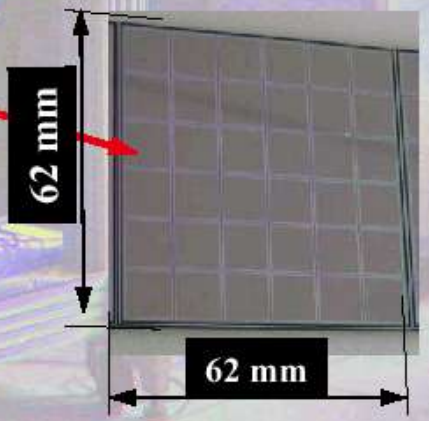
Note the density



- 3 structures W-CFi (1,2,3 x1.4mm)
- 15 « detector slabs »
- Dimension 200x360x360 mm

→ *9720 channels in prototype*

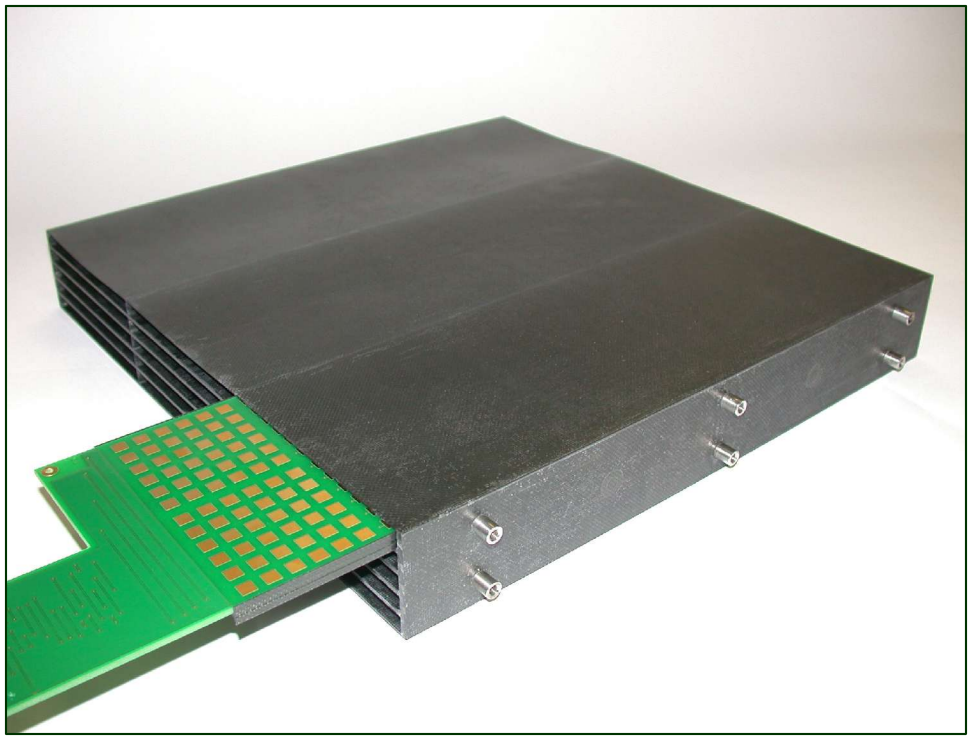
Silicon wafers with 6×6 pads (10×10 mm²)

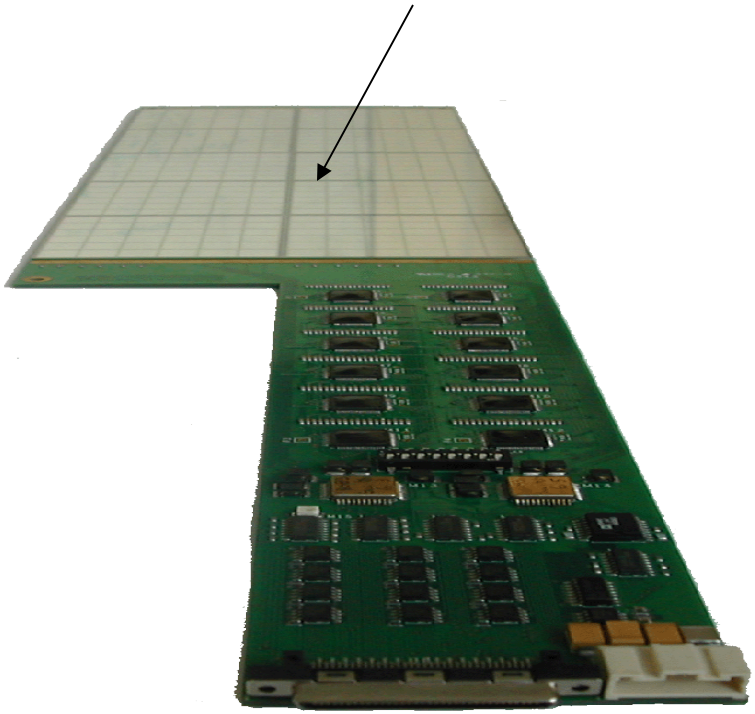


First stack elements

Wafers: Russia/MSU and Prague/IOP

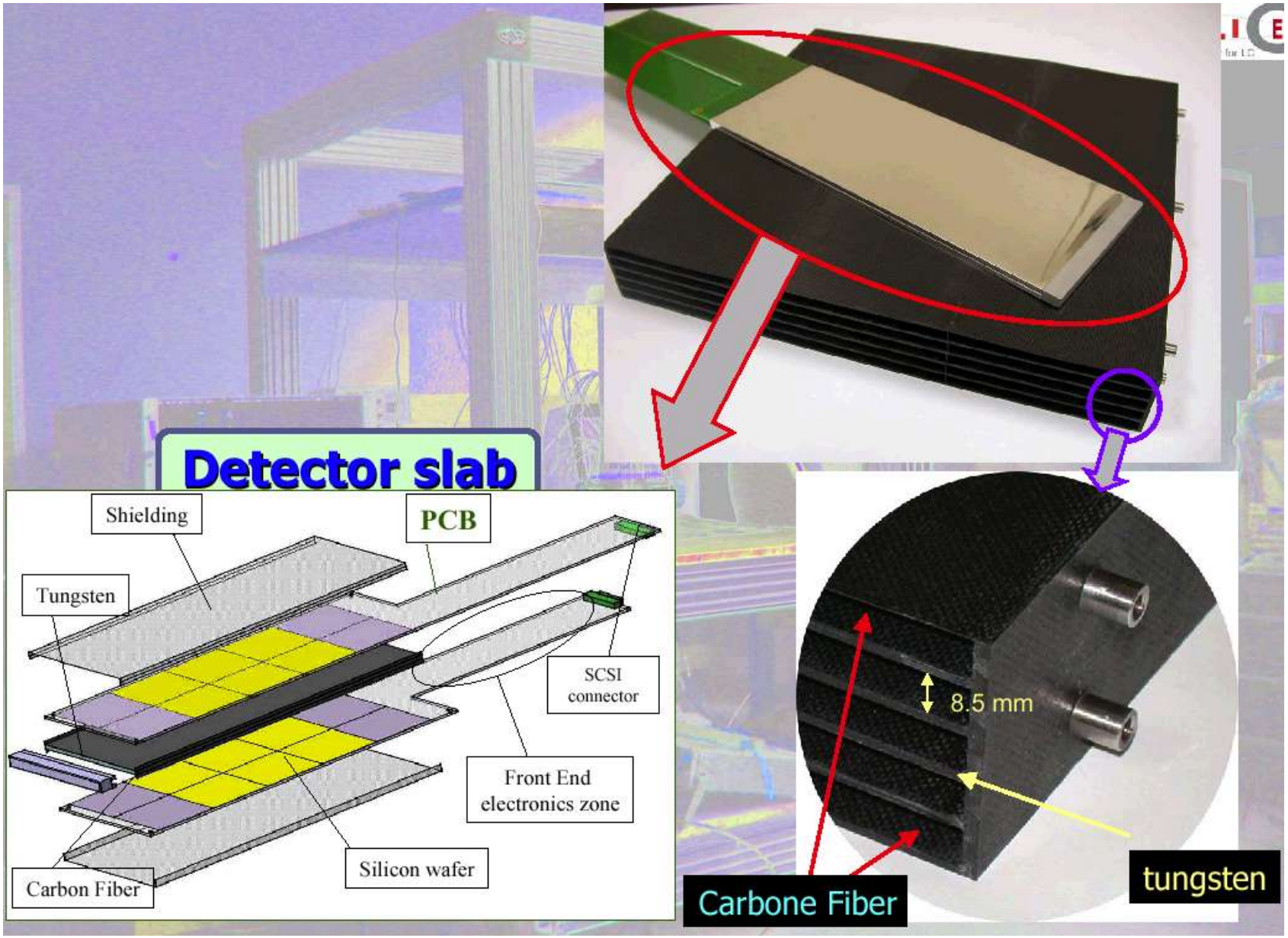
First structure from LLR





PCB: LAL design, production – Korea/KNU

Detector slab details



ECal – Si Wafers for Prototype

4″ High resistive wafer : 5 KΩcm

Thickness : 525 microns ± 3 %

Tile side : 62.0 + 0.0
- 0.1 mm

Guard ring

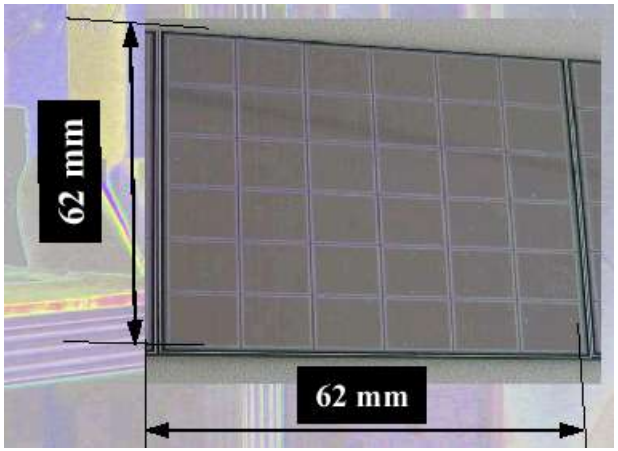
In Silicone ~80 e-h pairs / micron ⇒ 42000 e⁻ /MiP

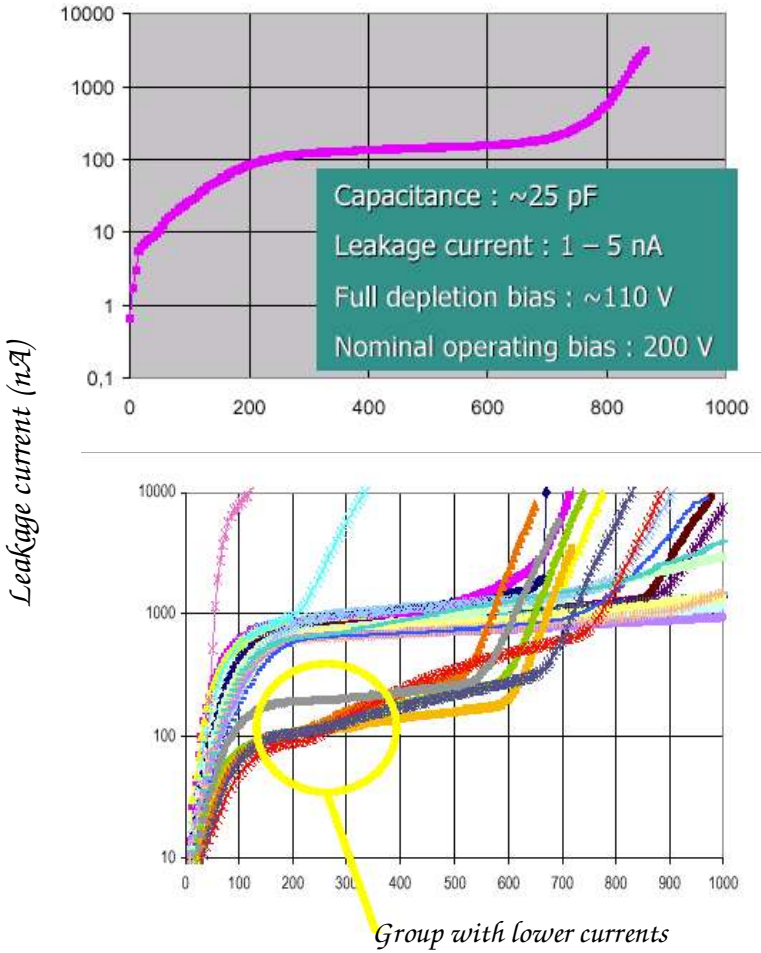
Capacitance : ~21 pF

Leakage current : 5 – 15 nA

Full depletion bias : ~150 V

Nominal operating bias : 200 V





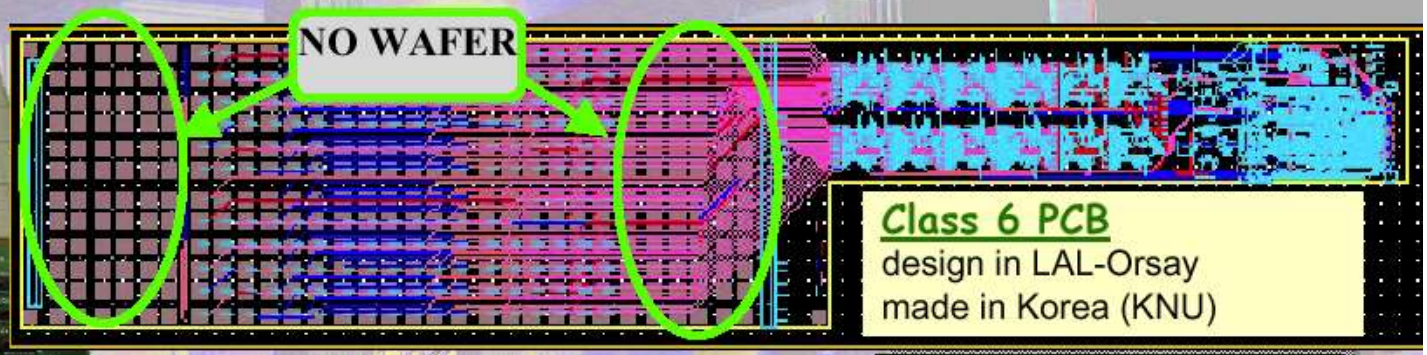
270 wafers needed:

~150 produced by MSU

~150 in prod. by IOP/Prague

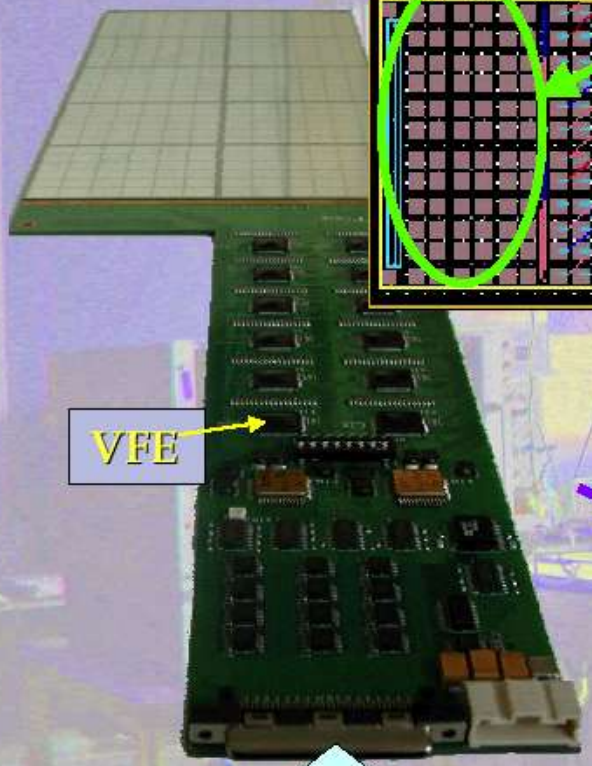
Silicon matrix

PCB for the prototype



Class 6 PCB
design in LAL-Orsay
made in Korea (KNU)

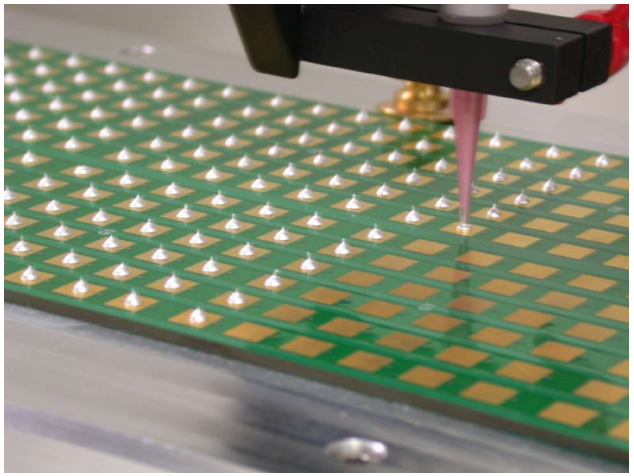
14 layers, 2 mm



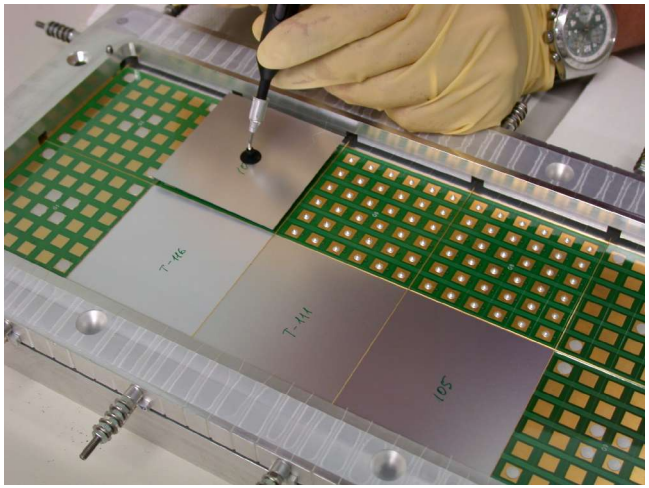
VME/PCI

Prototype : 60 PCB → middle of July

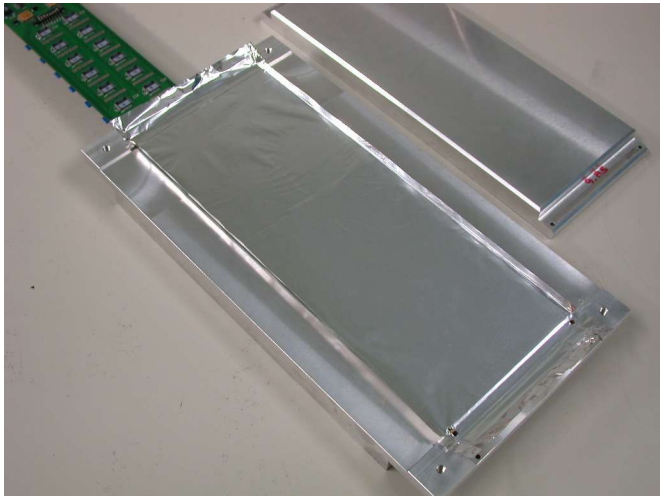
Some details of ECal prototype assembly



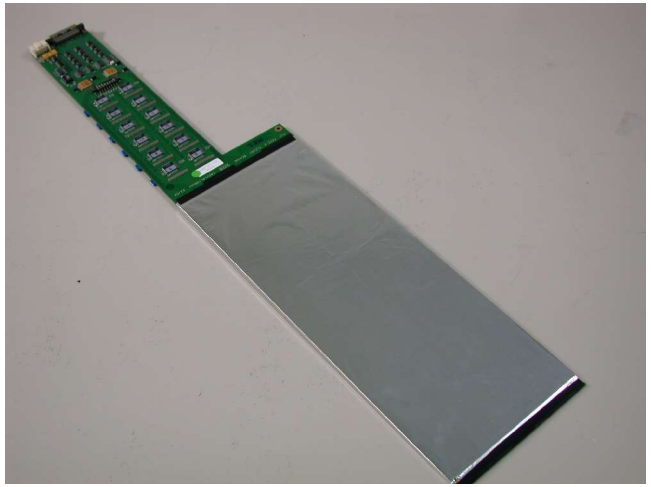
Applying conductive glue



Placing wafers on PCB



Wrap in aluminum foil – connect wafers to PCB ground (conductive EPO-TEK glue)



Finished PCB – ready to start production (two days/PCB)

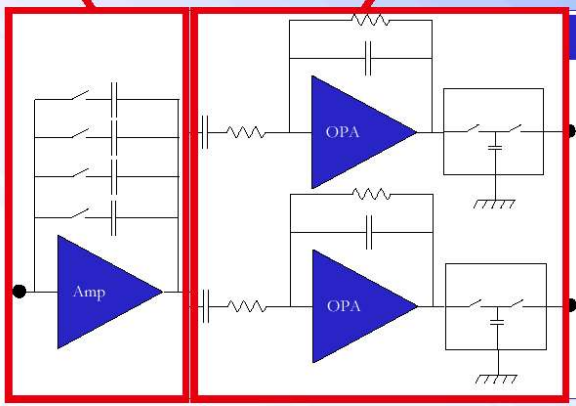
Front-end electronics for the prototype

LAL-Orsay

FLC_PHY3 overview

Multi-gain charge preamp
- 4 bits for gain selection
- Gain from 0.3 to 5 V/pC
- Gain selected offline

Dual shaper & track and hold
- Gain 1 and gain 10
- Work in parallel to select gain *a posteriori*



Global characteristcs
- 18 channel input
- 1 mux output

5

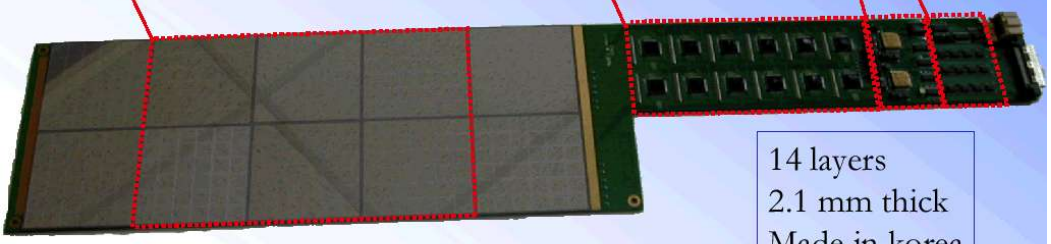
Presentation of the front-end electronic

6 active wafers
Made of 36 silicon PIN diodes
→ 216 channels per board
Each diode is a 1cm² square

2 calibration switches chips
6 calibration channels per chip
18 diodes per calibration channel

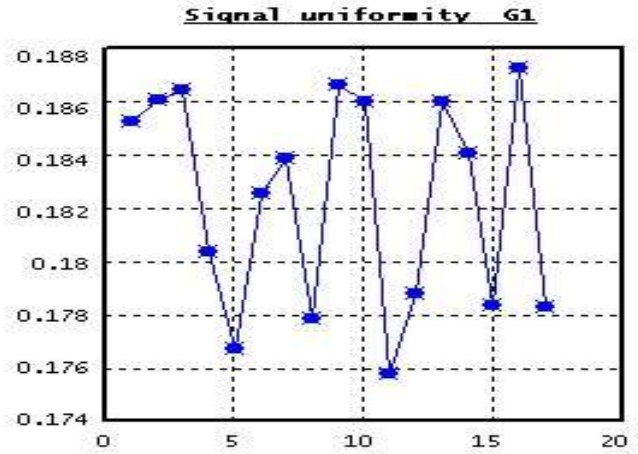
12 FLC_PHY3 front-end chip
18 channels per chip
13 bit dynamic range

Line buffers
To DAQ part
Differential



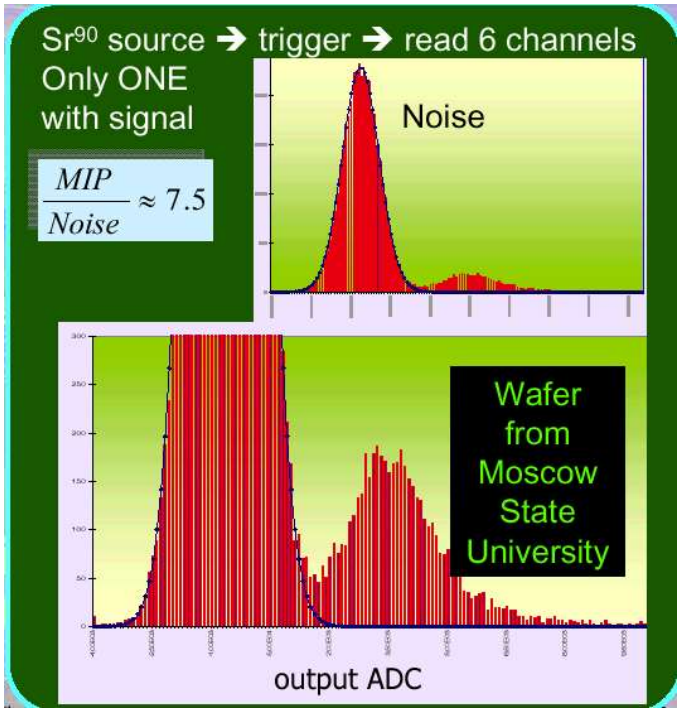
14 layers
2.1 mm thick
Made in korea

4



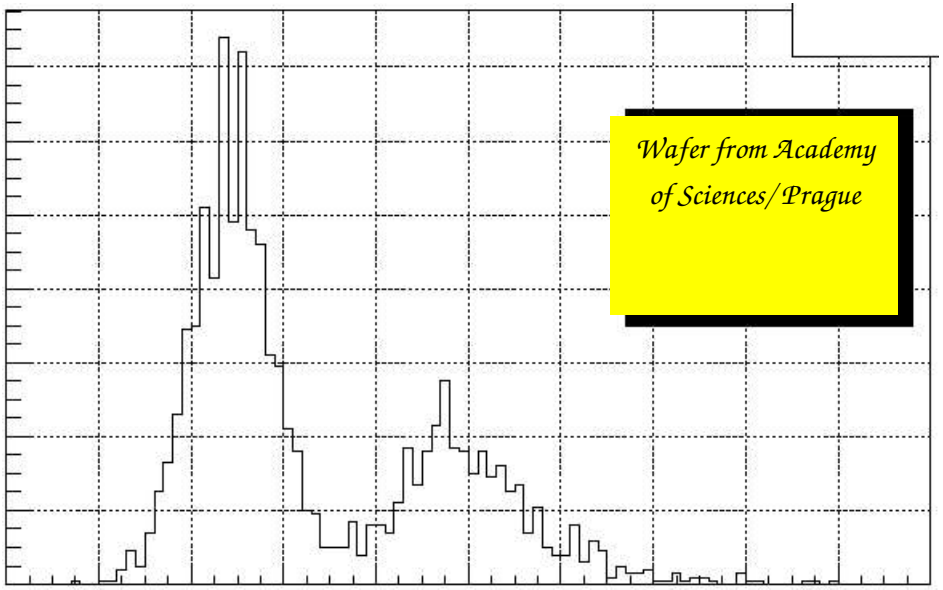
FLC_PHY3 production done

First results with complete detector slabs

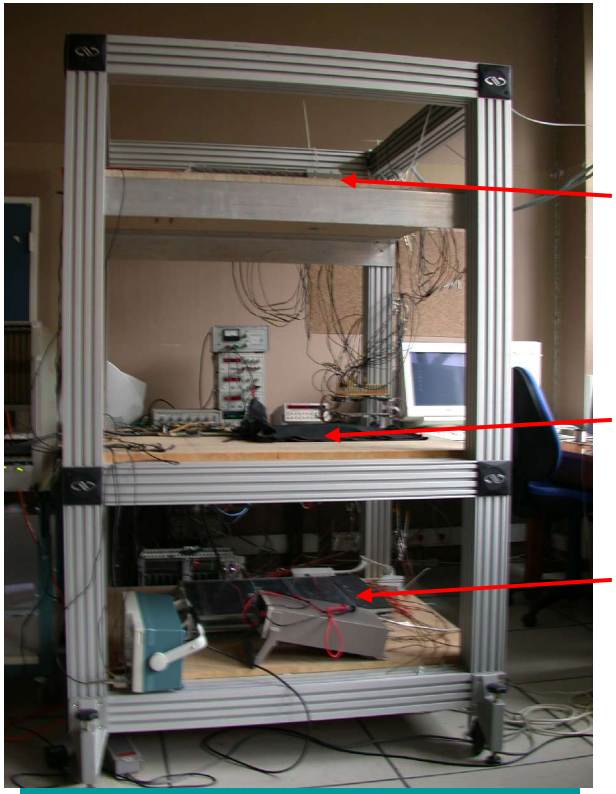


First results from source

Sr^{90} source -> trigger -> read 1 channel



Cosmic test bench at LLR



The cosmic test bench at LLR

Upper x and y planes of hodoscope

Silicon

Lower x and y planes of hodoscope

XY plane : 16x16 scintillators

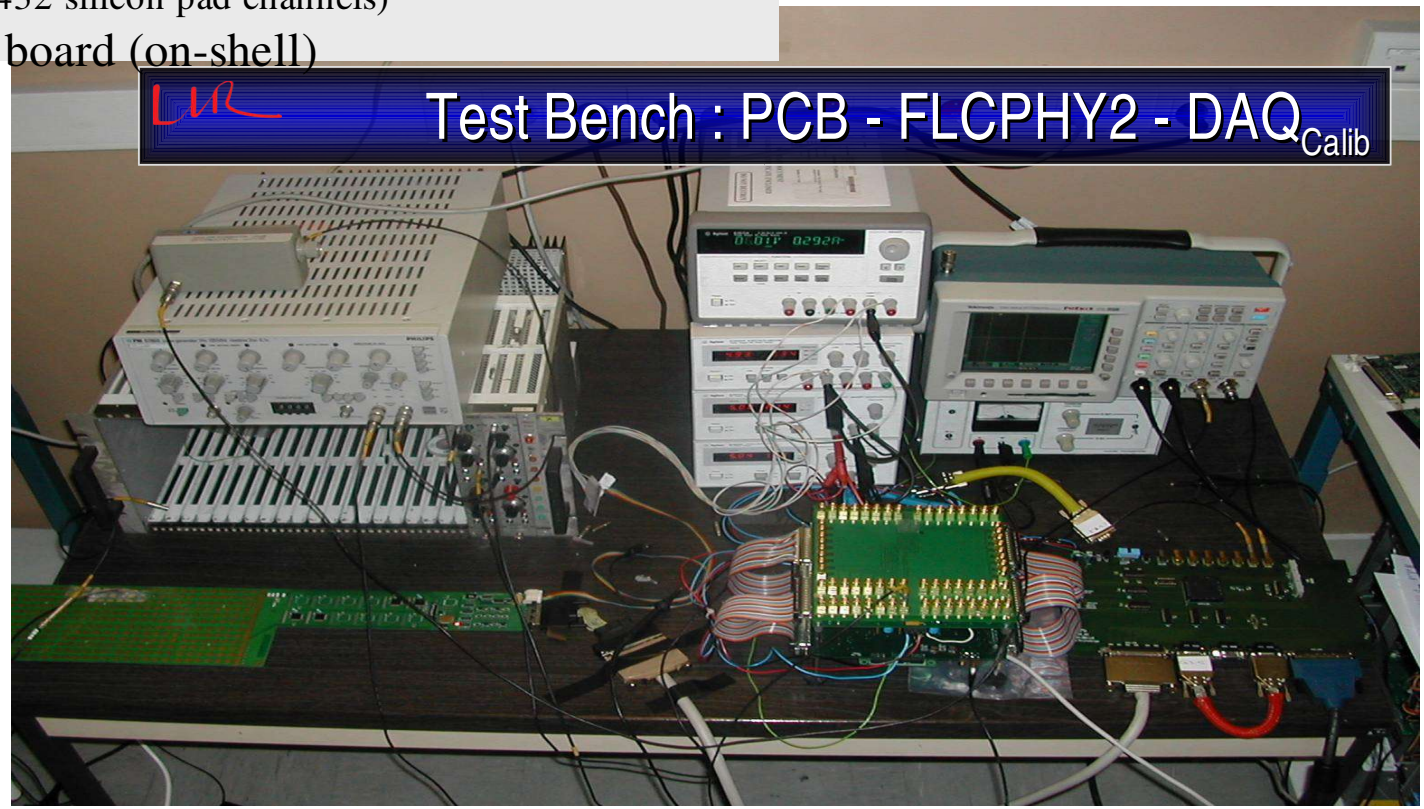
Active area : 44x44 cm²

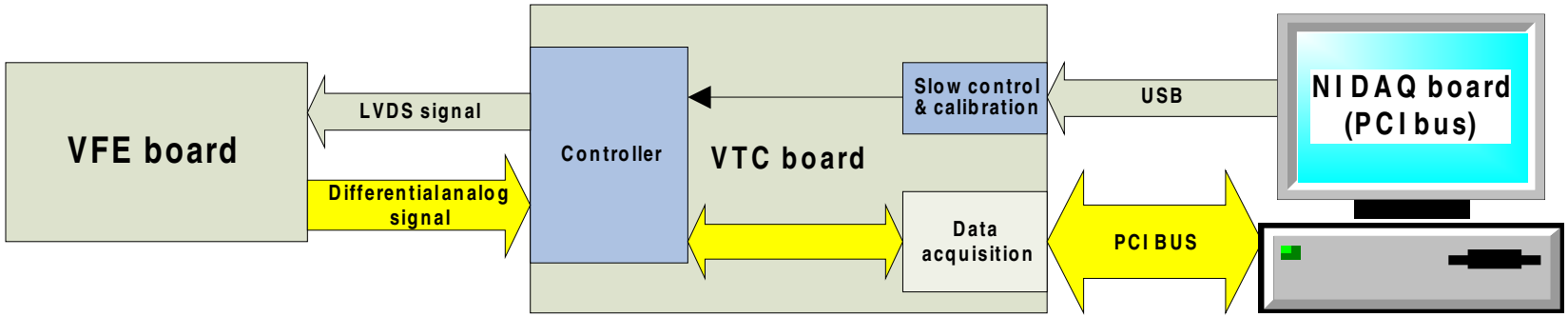
Cosmic Rate : ~ 1 Hz

"good" event : 90 %

Single Slab DAQ (SSD)

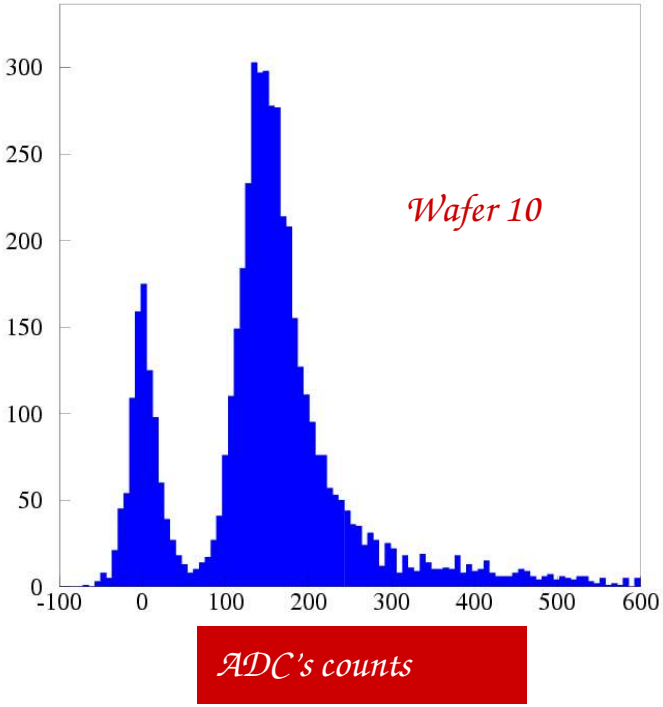
? for calibration and test on Cosmic Test bench
work only for a single detector slab
(24 VFE chips/ 432 silicon pad channels)
based on NI board (on-shell)

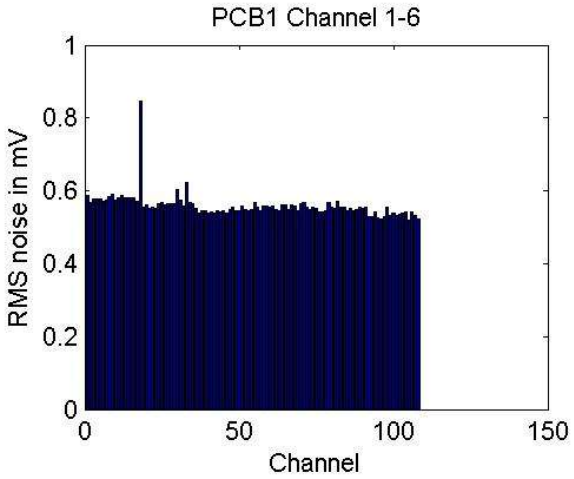


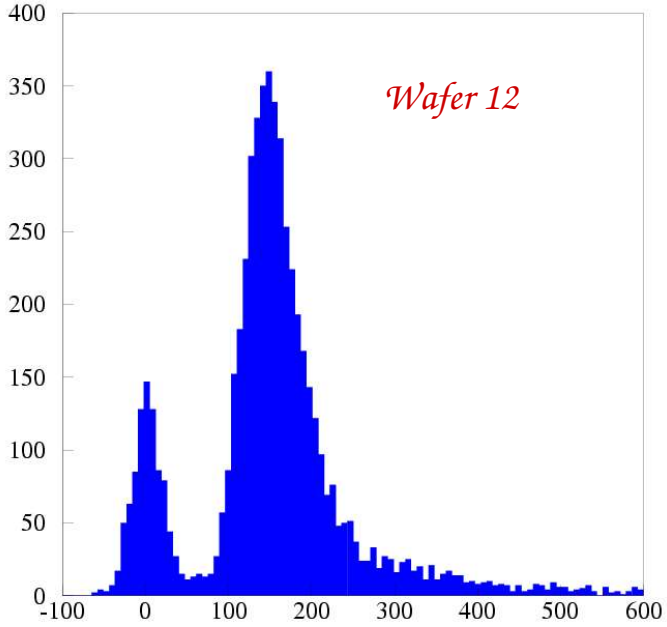


Results from

Cosmics/Single Slab DAQ



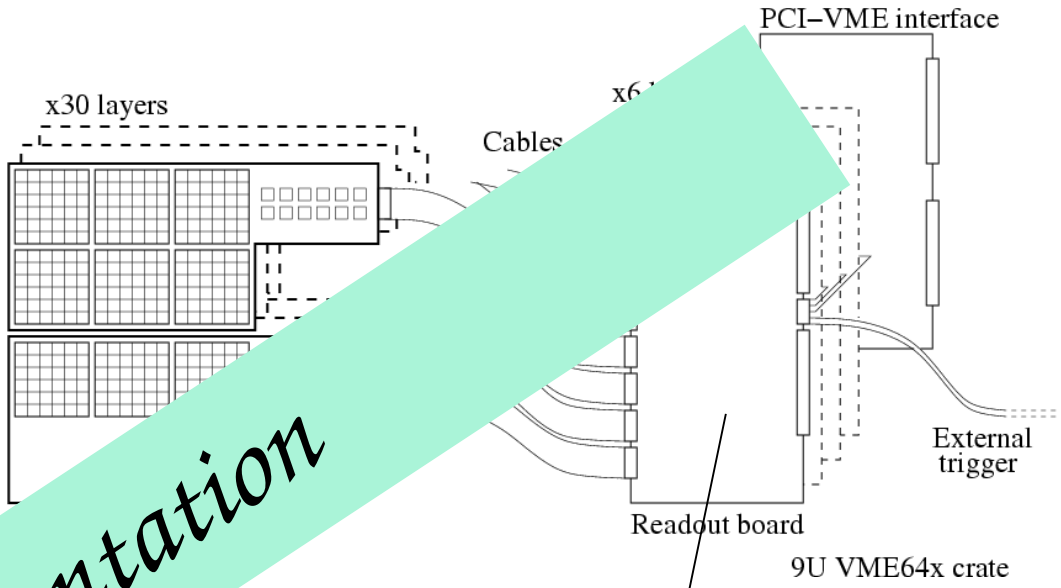




$$Mip/Noise = \frac{150}{19.5} \approx 7.7$$

NEED ~ 24 hours to calibrate one slab with a precision of about few per mill

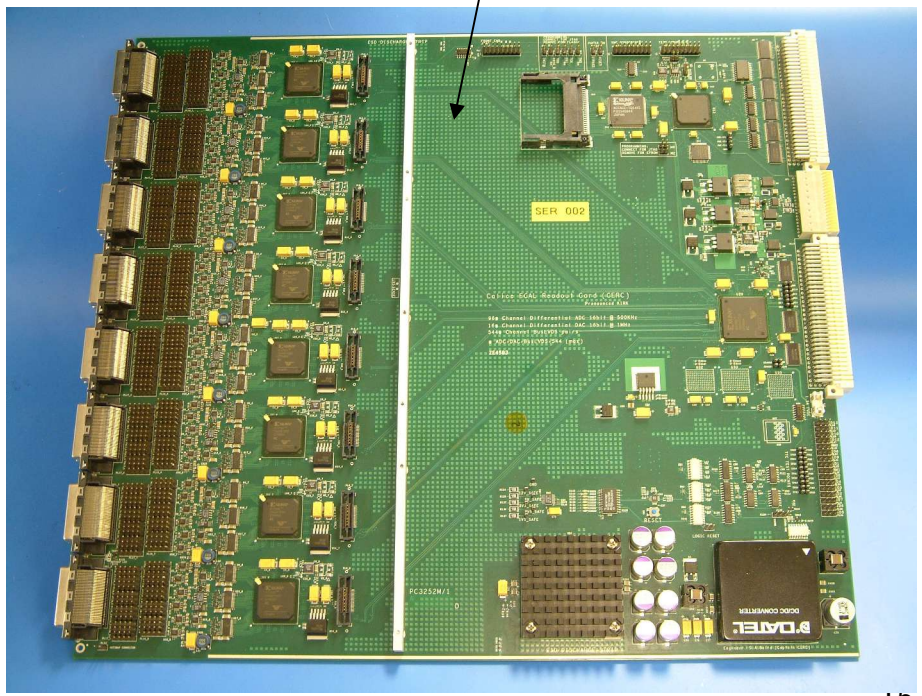
DAQ for ECAL Prototype



- Eight Front End (FE) FPGAs control all signals to front end electronics via front panel input connectors
- Back End (BE) FPGA gathers and buffers all event data from FE and provides interface to VME
- Trigger logic in BE backplane di… active i…
- Each … two half-full VFE … ed 45 inputs = 6 CERCs

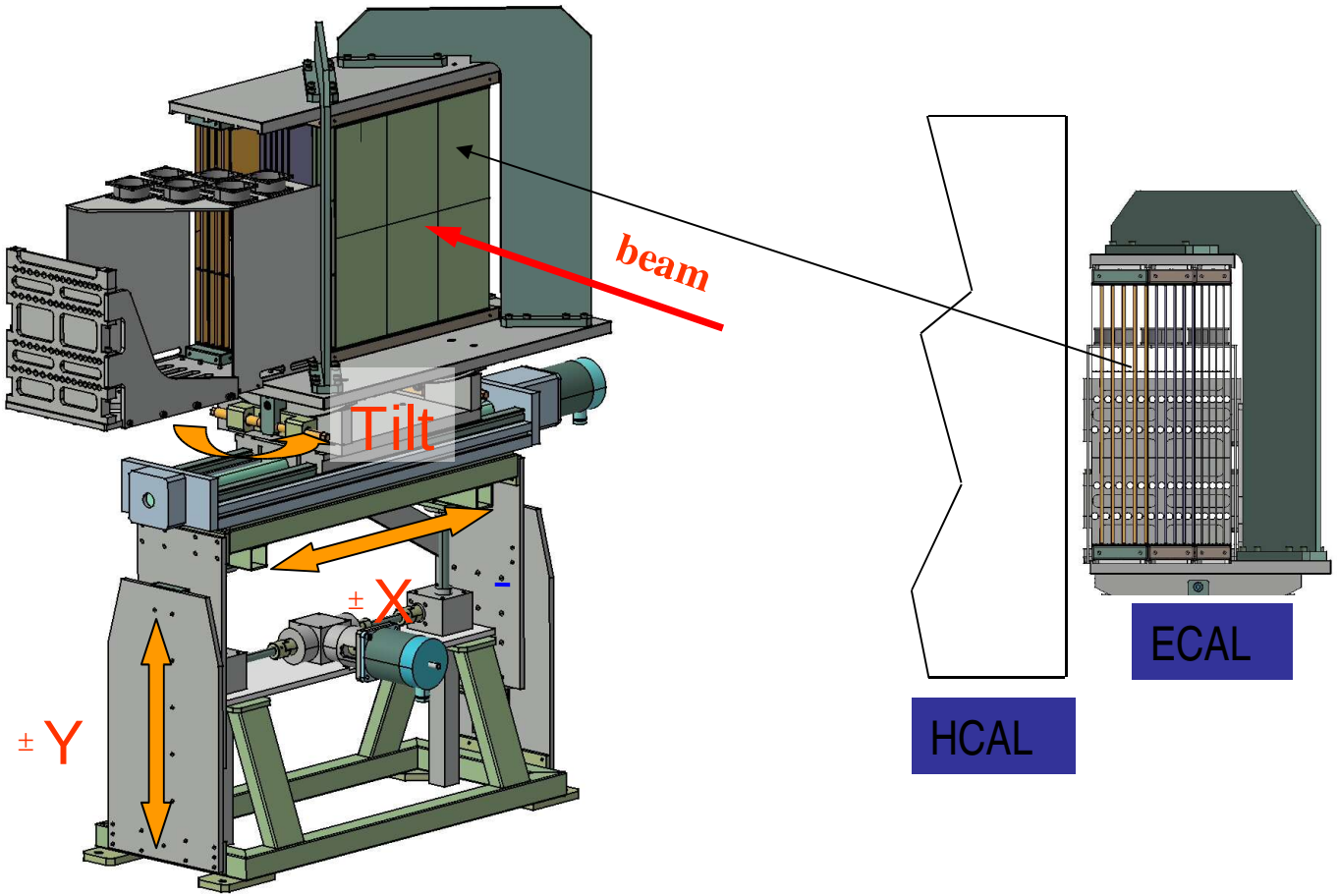
SEE Dan's presentation

The CERC



Preparations for test beam

…DESY late 2004



ECal Summary/Future

- A lot of progress !

- All items required for first full prototype are in hand or in production.

- Objective: exposure of first full prototype to low energy electron test-beam at DESY before the end of 2004.

- Future: expose prototype to higher energy electron beam, and hadron beam at FNAL/IHEP in combination with HCal prototypes (various options).