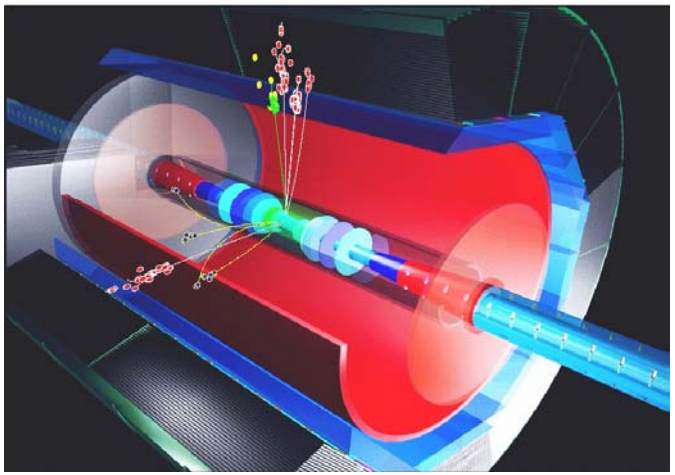
# Status of MAPS activities at DESY

Devis Contarato – DESY/Hamburg University



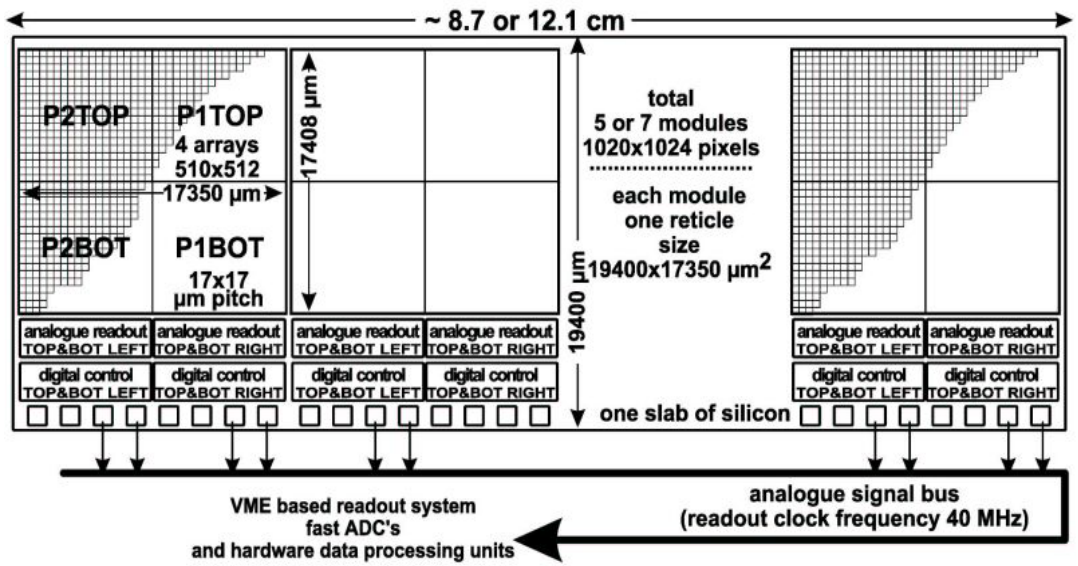
2nd ECFA Study Workshop – Physics and Detectors for a Linear Collider
University of Durham, 1-4 September 2004

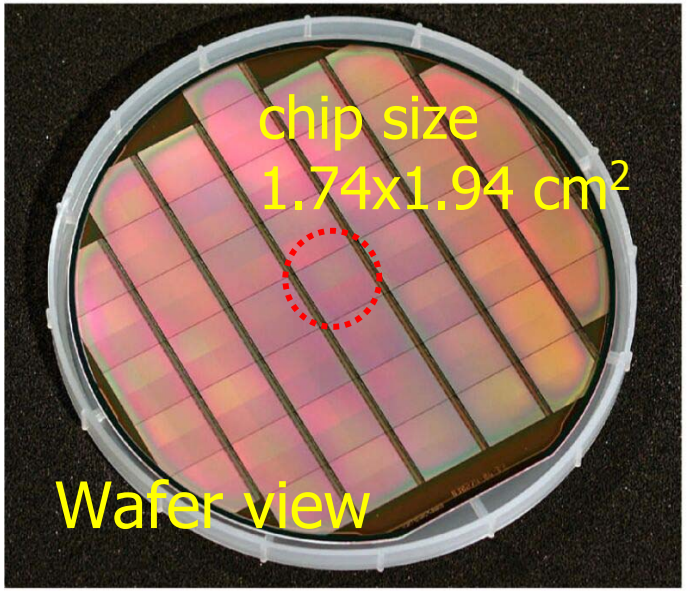
**On behalf of the DESY MAPS Group:**
V. Adler, D. Contarato, E. Fretwurst, T. Haas, J. Hauschildt, U. Kötz,
G. Kramberger, B. Löhr, P. Luzniak, C. Muhl, A. Polini, W. Zeuner

# DESY activities on MAPS

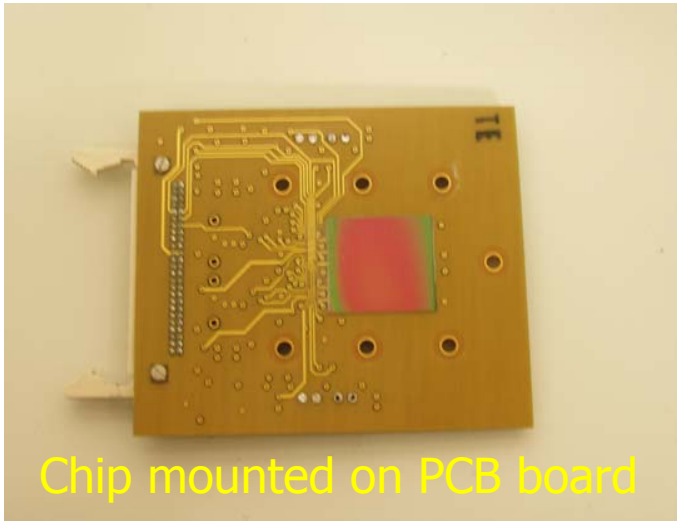
- Chip tests: test-beam with 6 GeV electrons at DESY
- Power consumption and cooling: simulations, tests
- Mechanical layout and support
- Power switching
- Physics simulations: optimization of VXD design

# MIMOSA V (B)

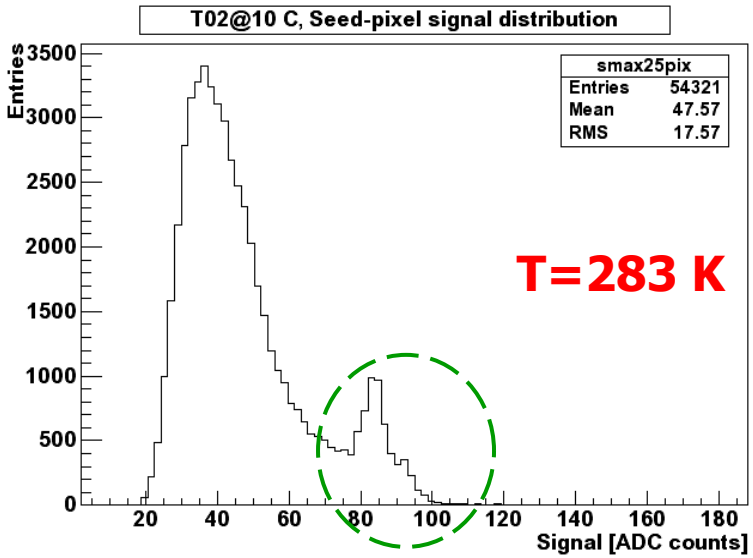


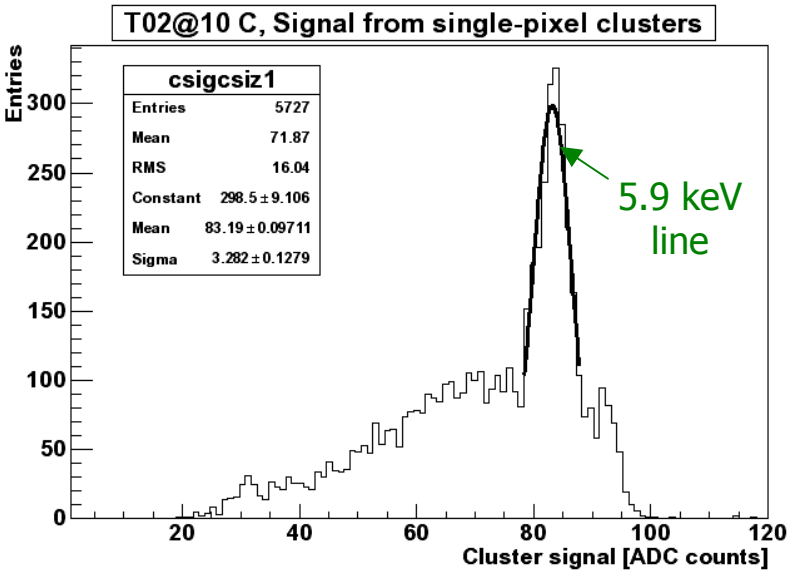



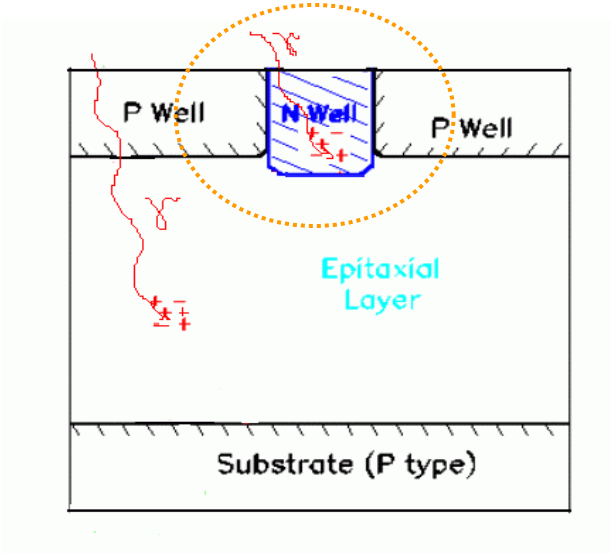

- real-size prototype: 3.5 $cm^2$, 1M pixels
- 2003 batch; improved fabrication process
- standard 0.6 µm CMOS of AMS with 14 µm epilayer
- pixel pitch 17x17 $\mu m^2$
- 4 independent matrices of 512x512 pixels
- serial analogue readout @ 10 MHz
- back-thinned down to 120 µm



# Calibration with $^{55}Fe$

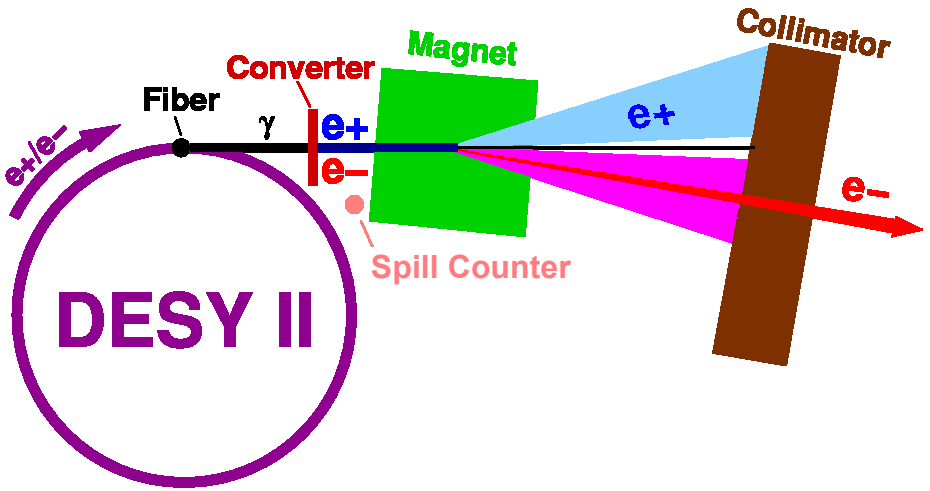


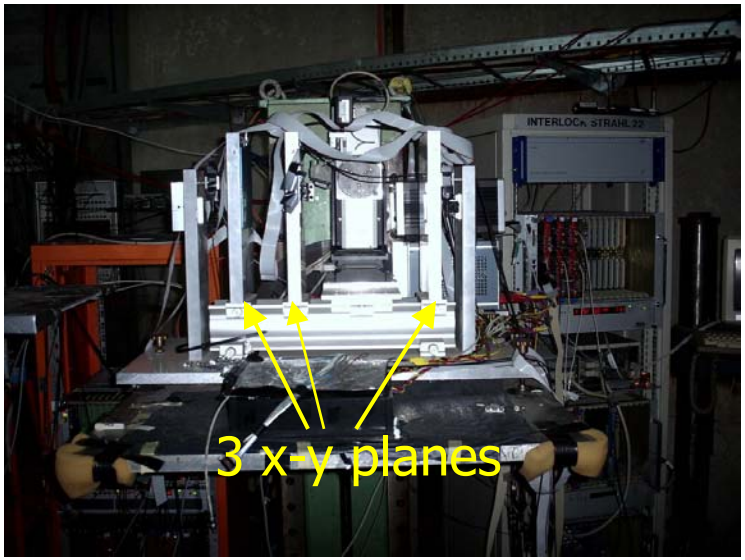



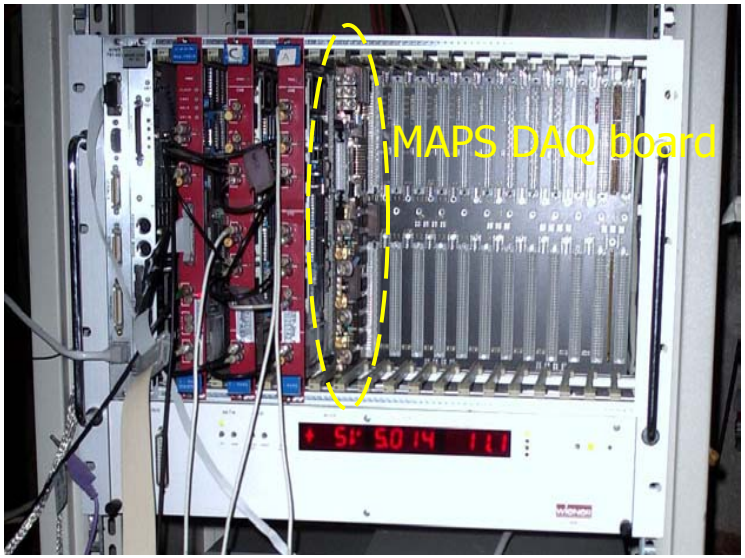




- Looking for conversion of the photon in the n-well diode (single pixel signal required, no signal on the neighbors).
- 5.9 keV peak used to calibrate noise
- conversion factor ~20 electrons/ADC
- average pixel noise ~3 ADC counts
- ENC ~40 electrons

# MAPS Beam-tests at DESY



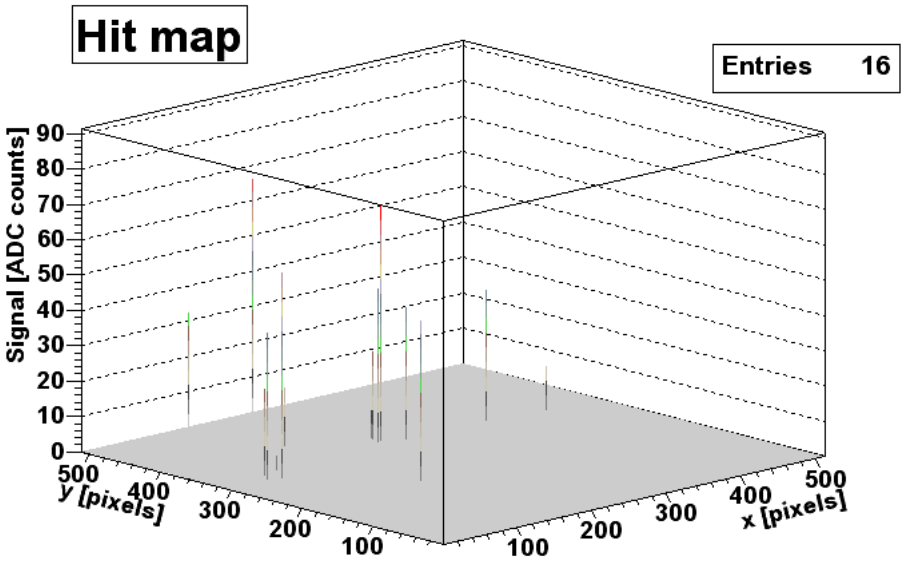




- electrons from 1 to 6 GeV
- event rate ~5 Hz for 1 $cm^2$
- 3 x-y planes silicon telescope (~10 μm)
- VME readout (Motorola PowerPC CPU)
- support for 2 Mimosa V chips available, cooling to –15°C possible
- Stand-alone readout software for detector and telescope

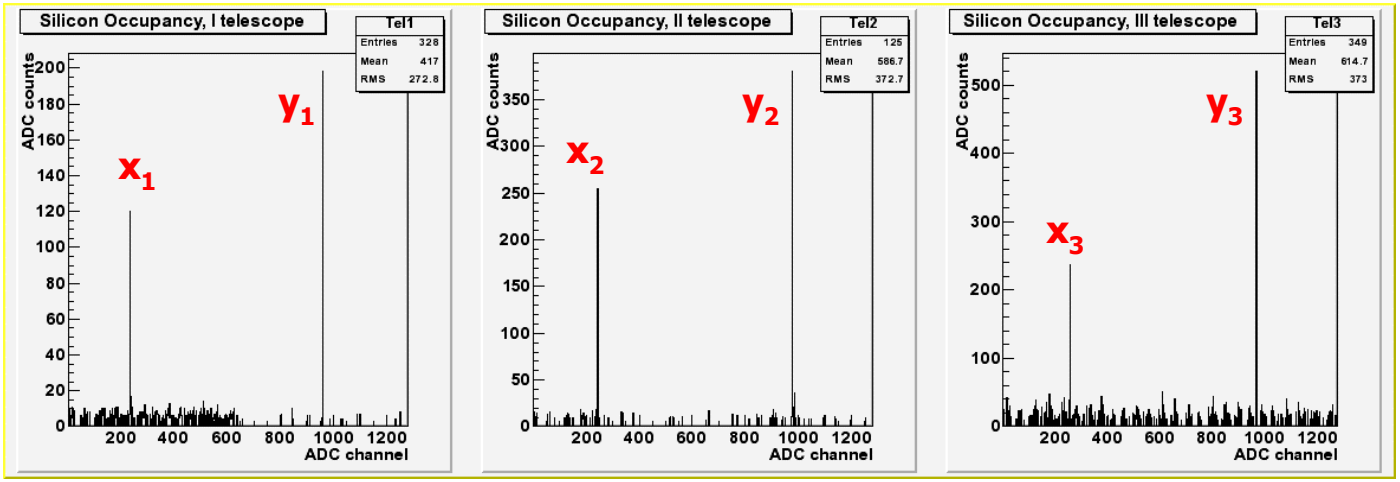
First tests: middle August 2004

- 2 matrices at 10°C and 0°C, ~13000 events

# Typical event

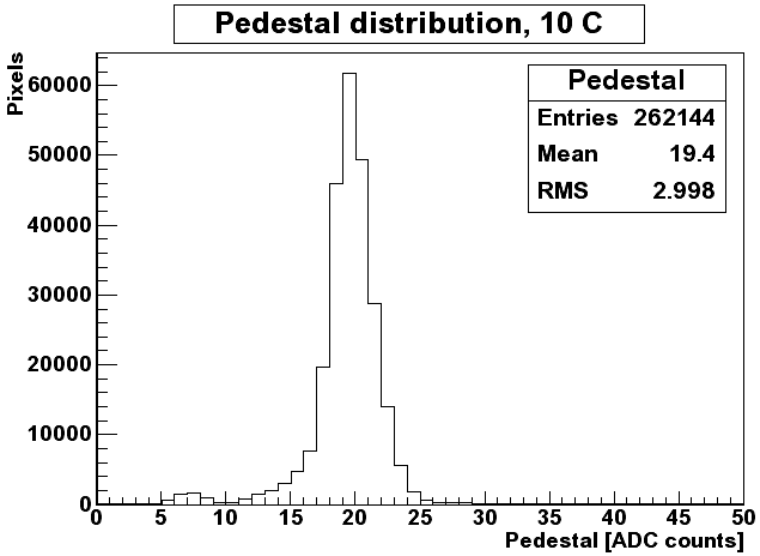


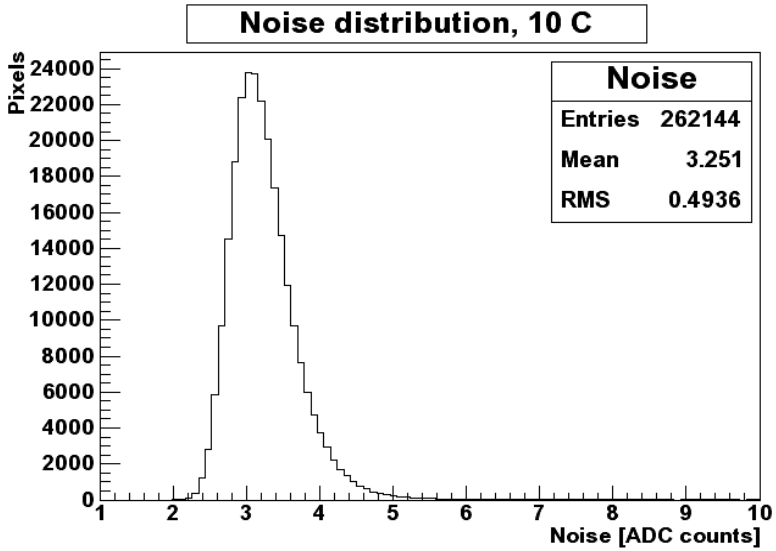

- High hit-occupancy for every event (detector integrates during VME dead-time)
- DAQ and data transfer/storage need to be improved to reduce hits/event
- Clustering software being developed from the one used for source runs
- Pattern recognition to find good hit

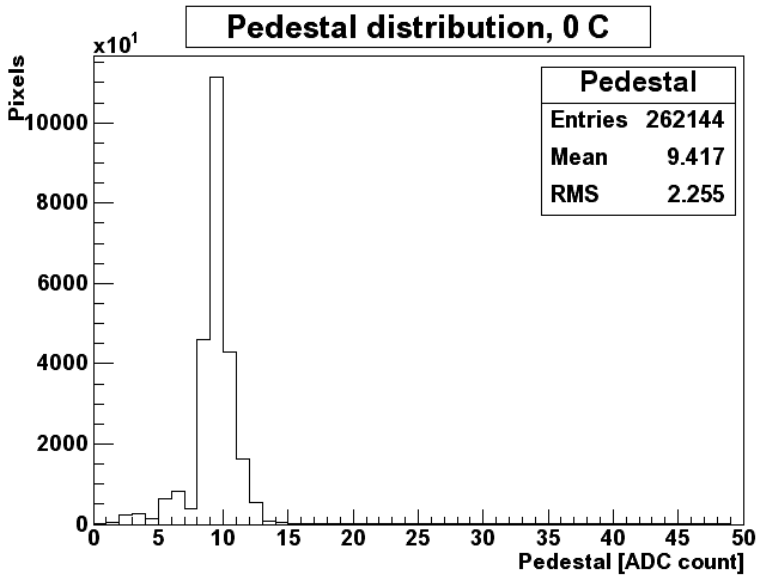


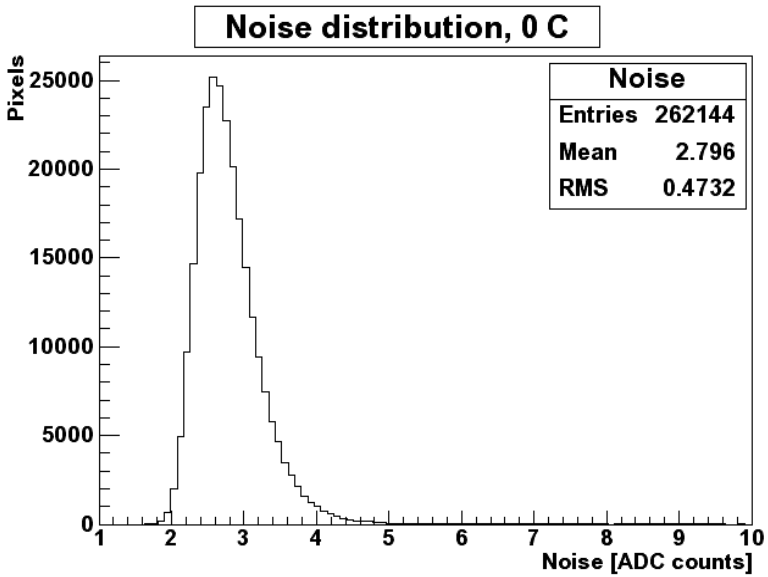

Example track from the telescope

# Noise and Pedestals

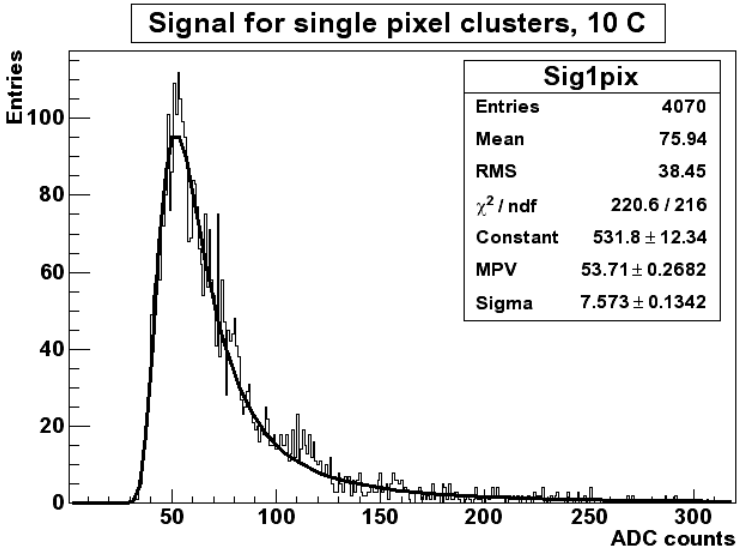


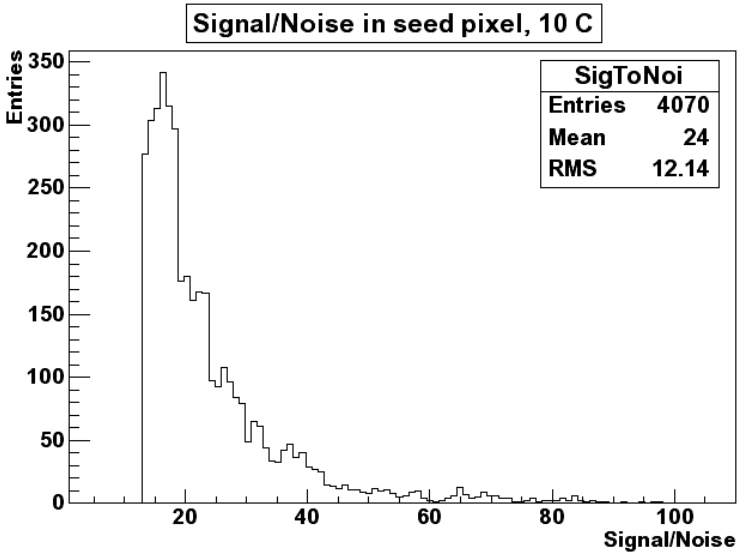



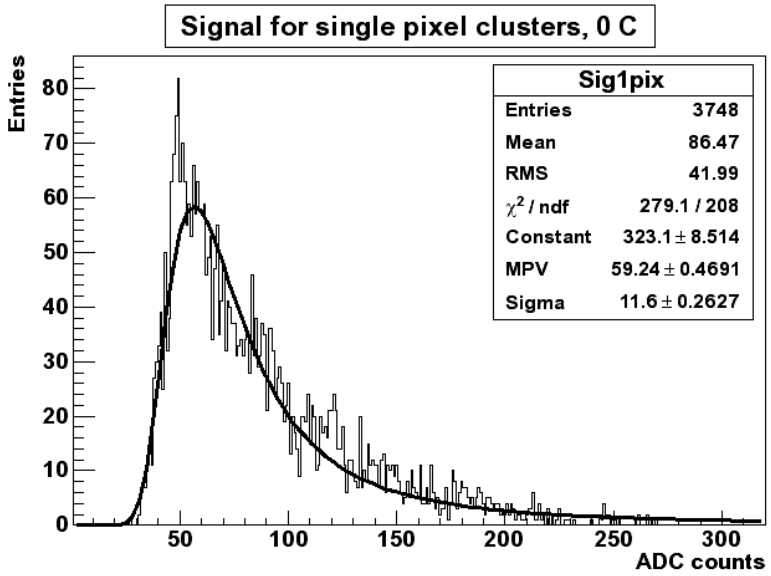



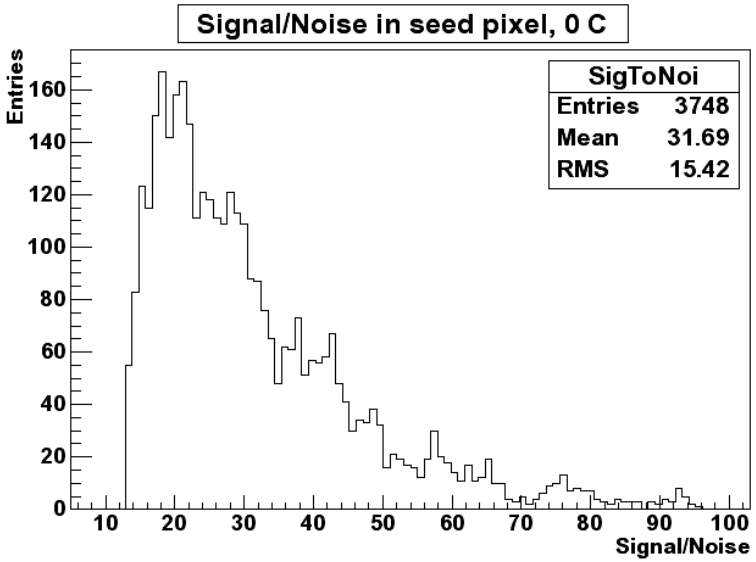



# Signal and S/N

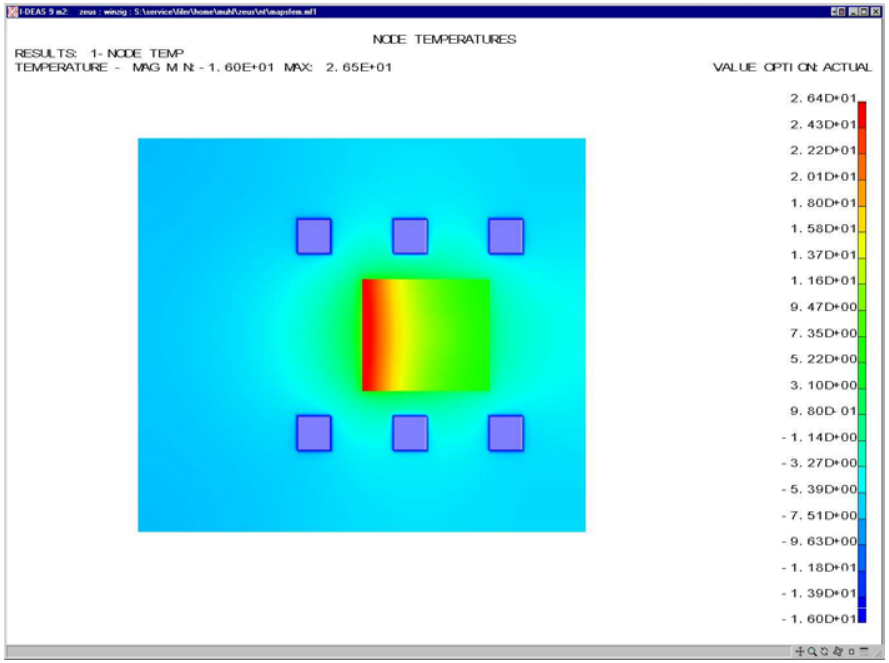


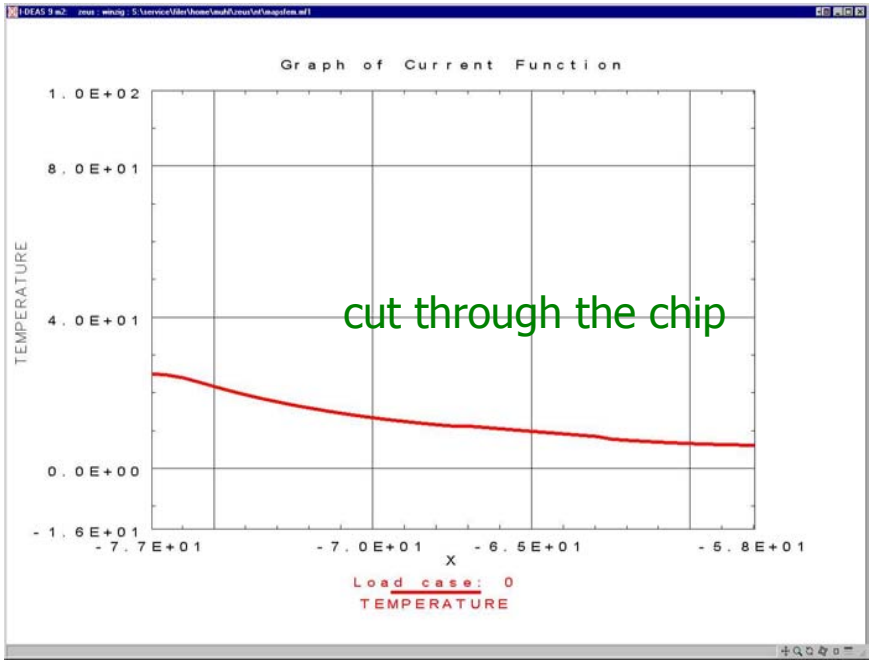



# Simulation of temperature distribution

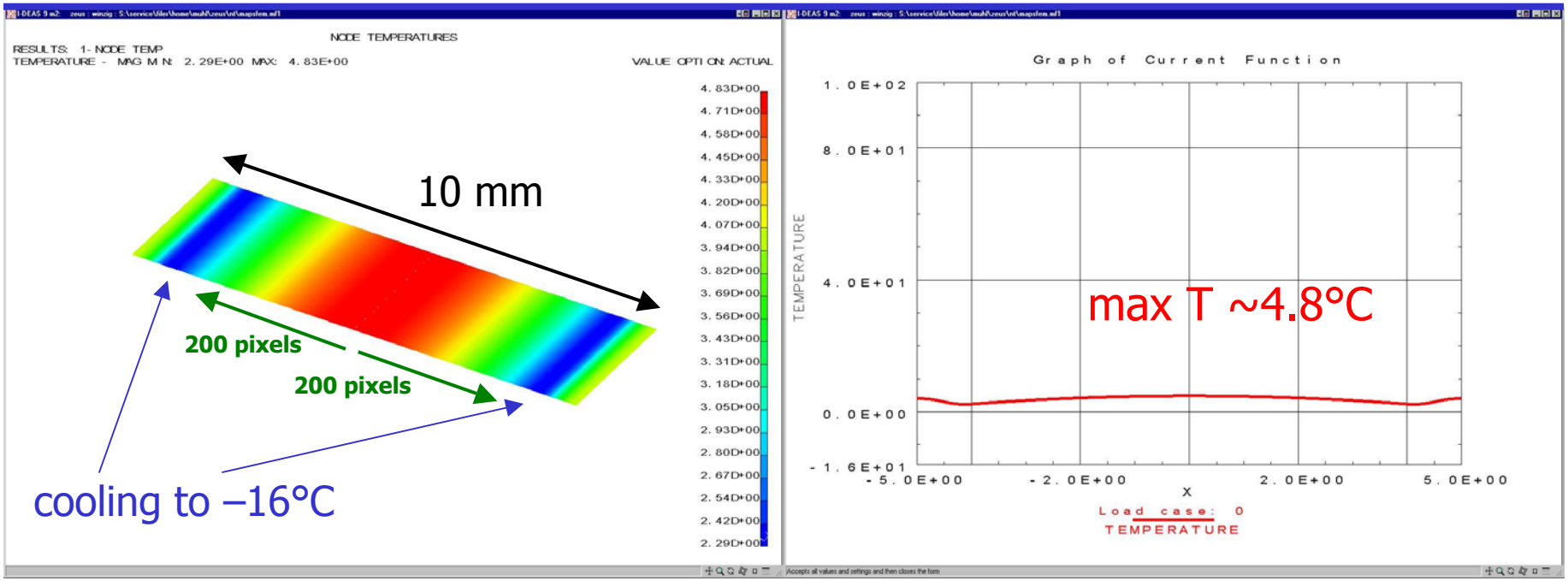



- simulation of cooling conditions in our experimental set-up
- Mimosa 5 chip in a brass box cooled down to -16°C, nitrogen flow
- Chip thickness 120 μm, PCB board modelled with a 0.035 mm copper layer
- Convective heat transfer coefficient $\alpha \sim 10$ W/m$^2$·K
- Temperature distribution simulated with I-DEAS®-TMG®
- Chip temperature varies from +26°C in the readout area to +6°C in the pixel area

(from Carsten Muhl, DESY)

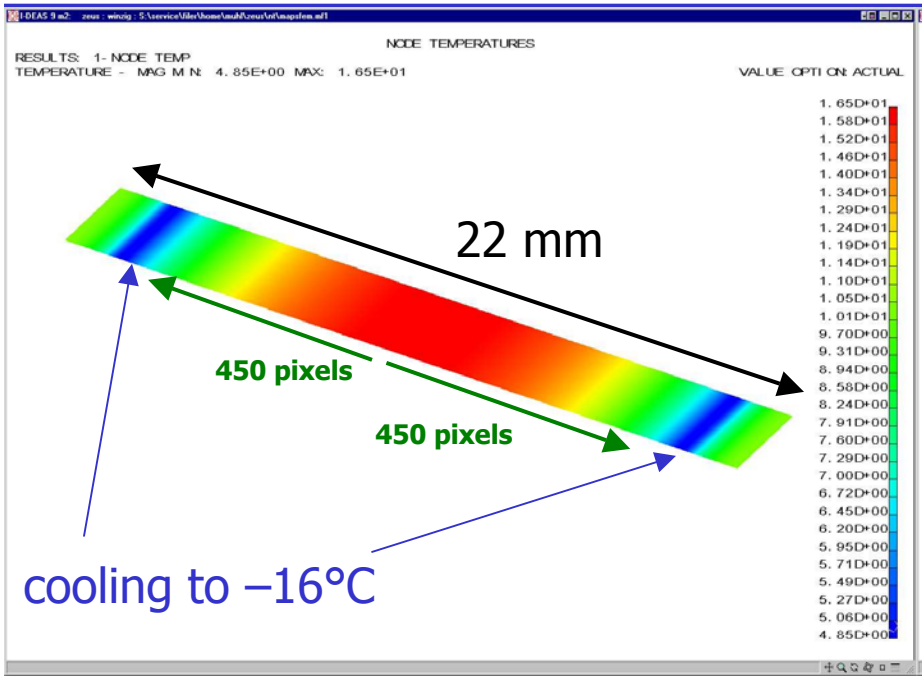
# Calculation for central VXD MAPS ladder

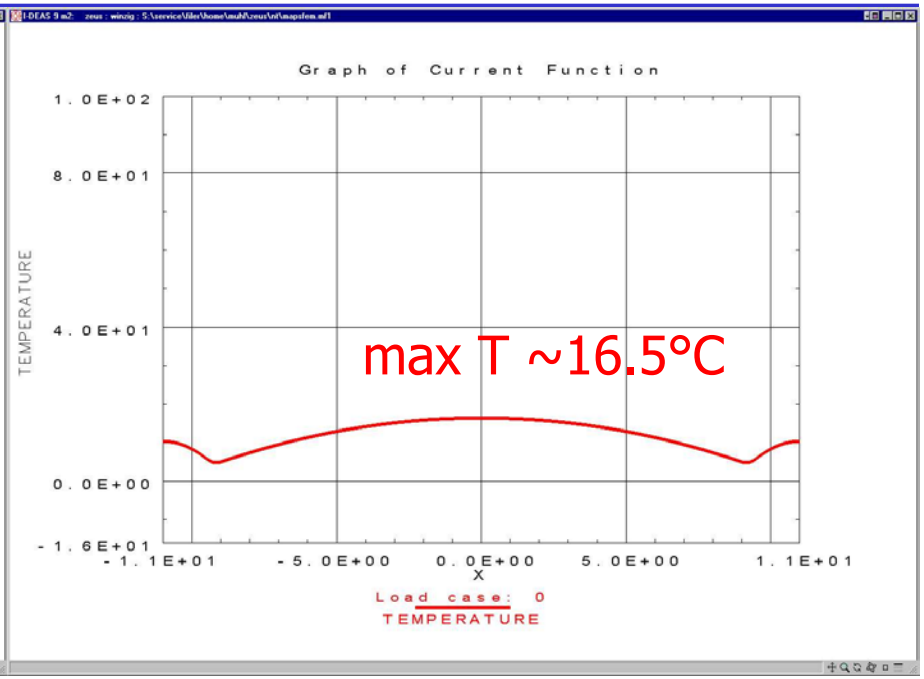



- 3 mm long portion of 10 mm wide ladder, 30 μm thick
- Thermal coupling: 2500 W/m$^2$K to a –16°C fluid, via two 0.5 mm wide strips on both sides of the bottom (a better coupling is feasible)
- No convective coupling to environment gas
- Under these conditions cooling is much better than for a single chip

(from Carsten Muhl, DESY)

# Calculation for outer VXD MAPS ladder

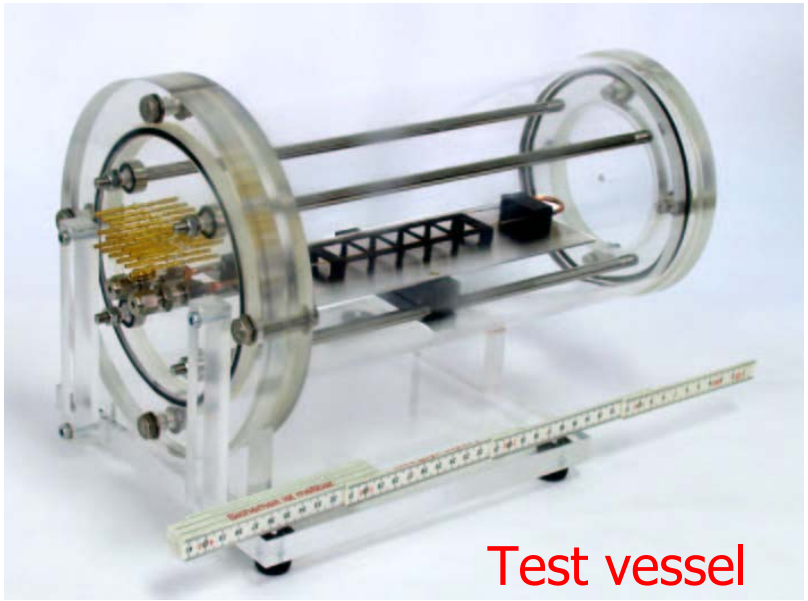


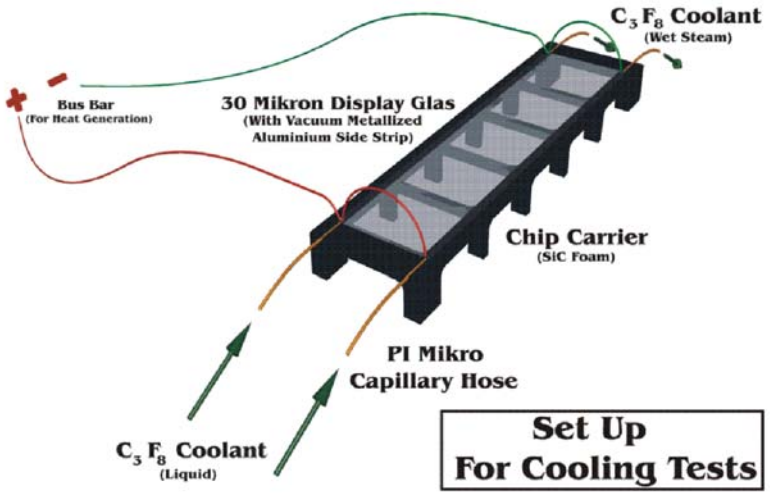




- 3 mm long portion of 22 mm wide ladder, 30 μm thick
- Thermal coupling: 2500 W/m$^2$K to a –16°C fluid, via two 0.5 mm wide strips on both sides of the bottom (a better coupling is feasible)
- No convective coupling to environment gas
- Higher maximum temperature than for central ladder
- Additional convection (not shown) would need additional cooling power

(from Carsten Muhl, DESY)

# Cooling tests



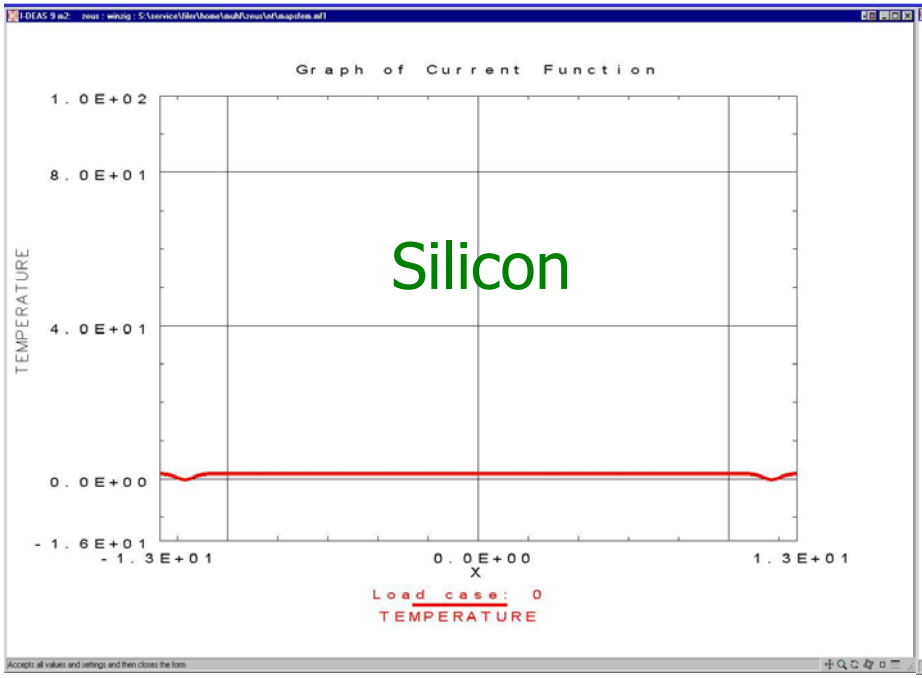



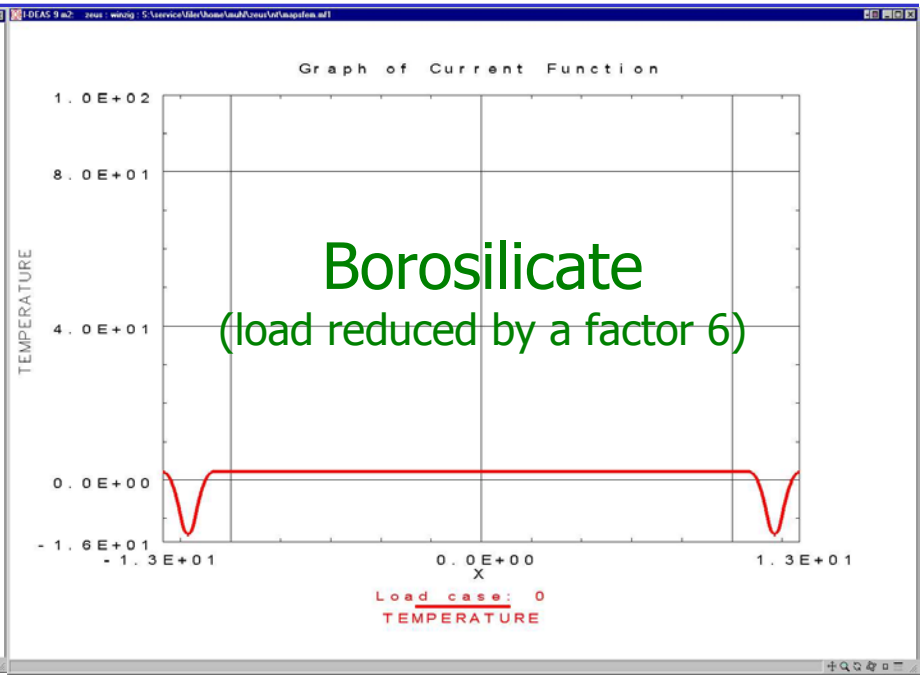


- evaporative cooling (like ATLAS) using octafluoropropane $C_3F_8$: cooling plant available
- vessel with 30 µm glass ladders (SiC foam support) and aluminum strips to simulate power dissipation, 300 µm capillaries for cooling liquid
- tests under way!

(from Jan Hauschildt, DESY)

# Use of display glass for cooling tests

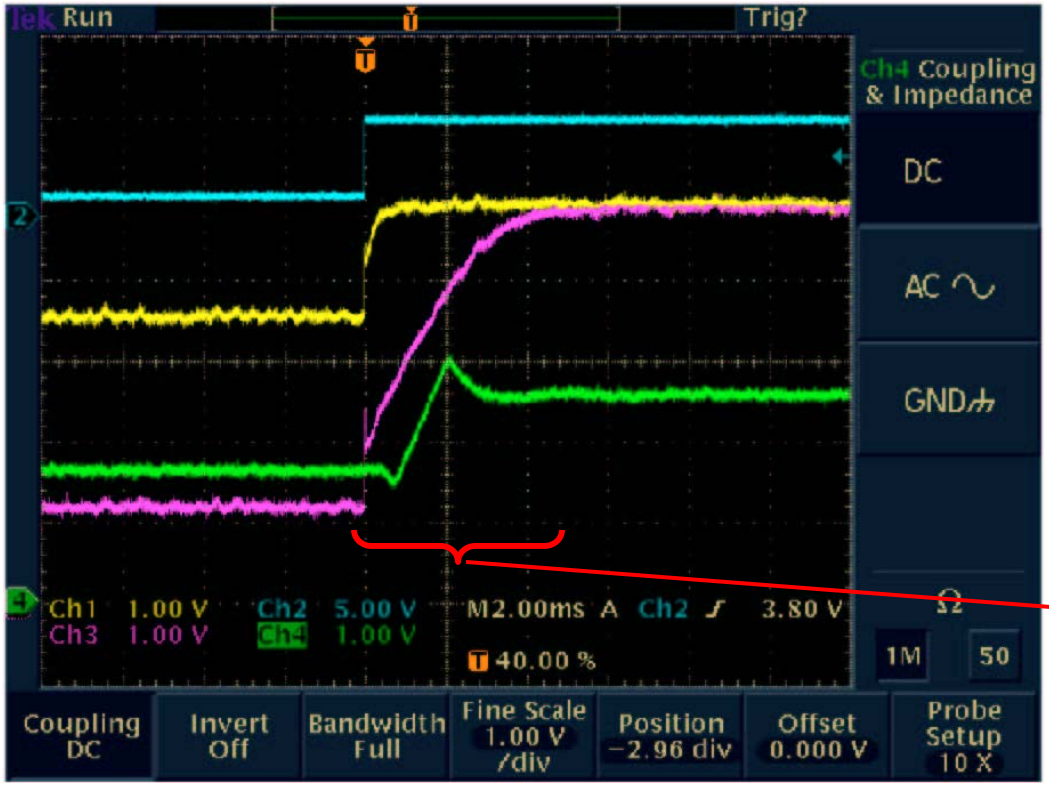



- Simulation of display glass test-ladder (25,4 mm x 102,4 mm x 0.03 mm), with two aluminum strips on both sides to represent readout area
- Conductivity of display glass worse than silicon (factor 6)
- Thermal coupling: 2500 W/m$^2$K to a –16°C fluid
- A temperature of ~2°C should be achieved in the pixel area

(from Carsten Muhl, DESY)

# Power switching




power switch

digital power line

analog power line

Mimosa 5 output

settling time within 4 ms

- principle has been proved (G. Claus, IReS-LEPSI, Strasbourg)
- facilities present on new version of control board
- tests under preparation

# Outlook

- **Test-beam schedule:**

  Fall 2004

  - extensive studies as a function of T (single matrix)
  - multiple matrices readout (2/4)
  - test of irradiated chip (900 MeV electrons, Trieste)

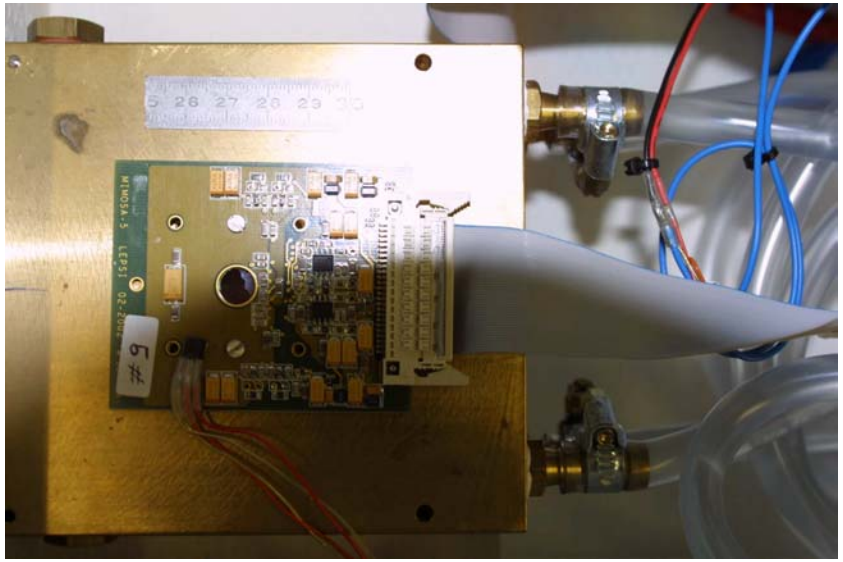
  2005

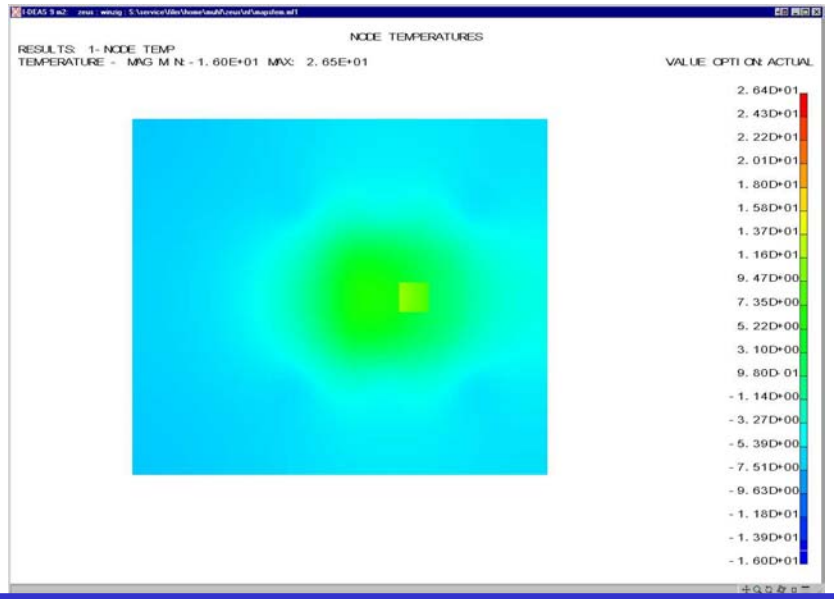
  - test of two Mimosa chips together (Maps telescope)
  - tests with || magnetic field (2 T) possible

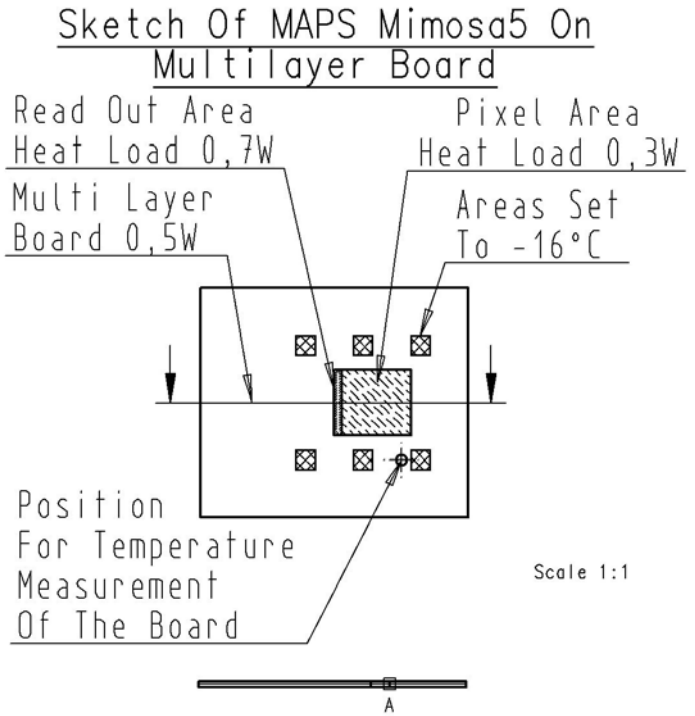
- **Cooling tests:** hardware available (vessel with dummy ladders and cooling plant), tests under way

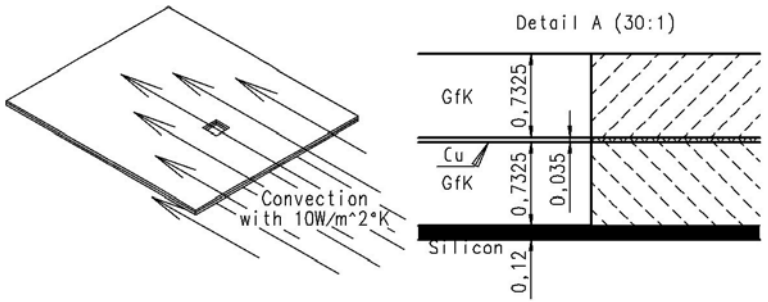
- **Power switching tests:** in preparation for next year

# Temperature simulation (2)



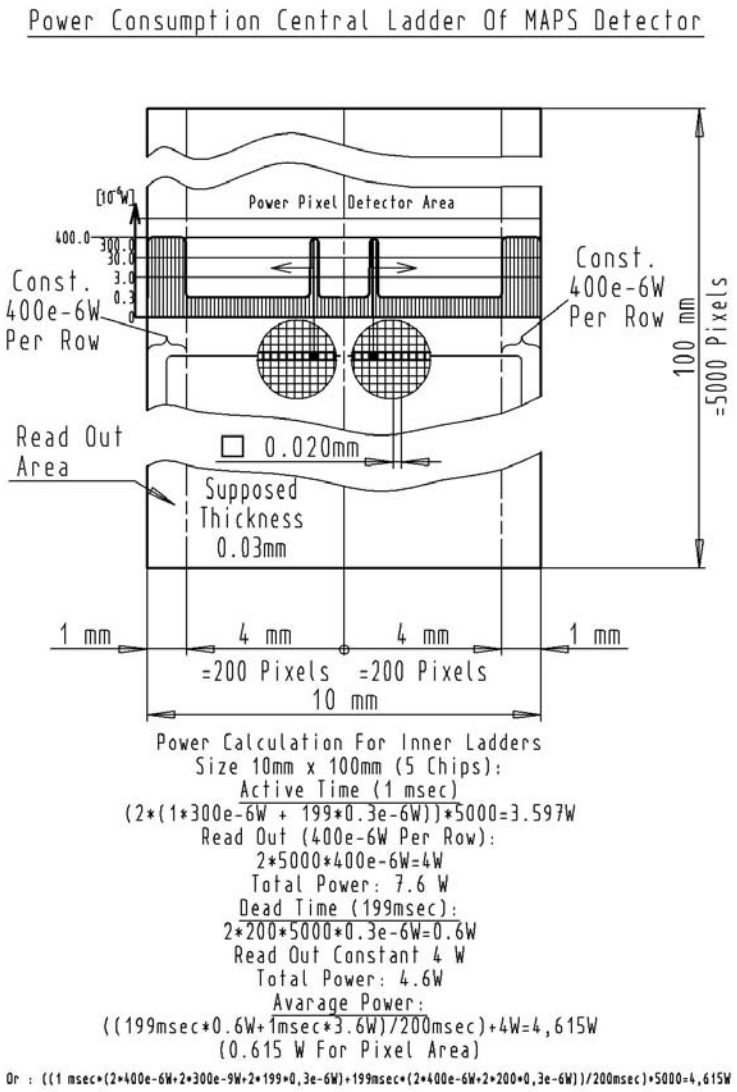


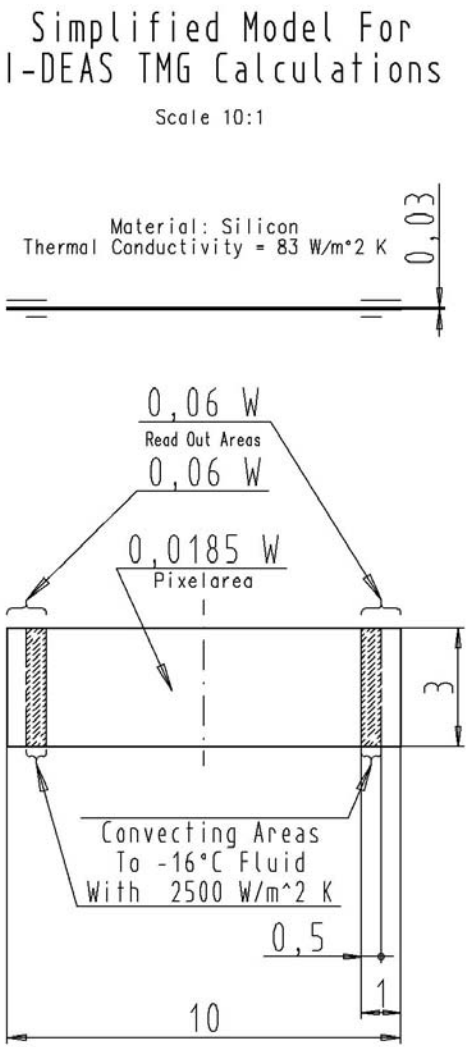




(from Carsten Muhl, DESY)

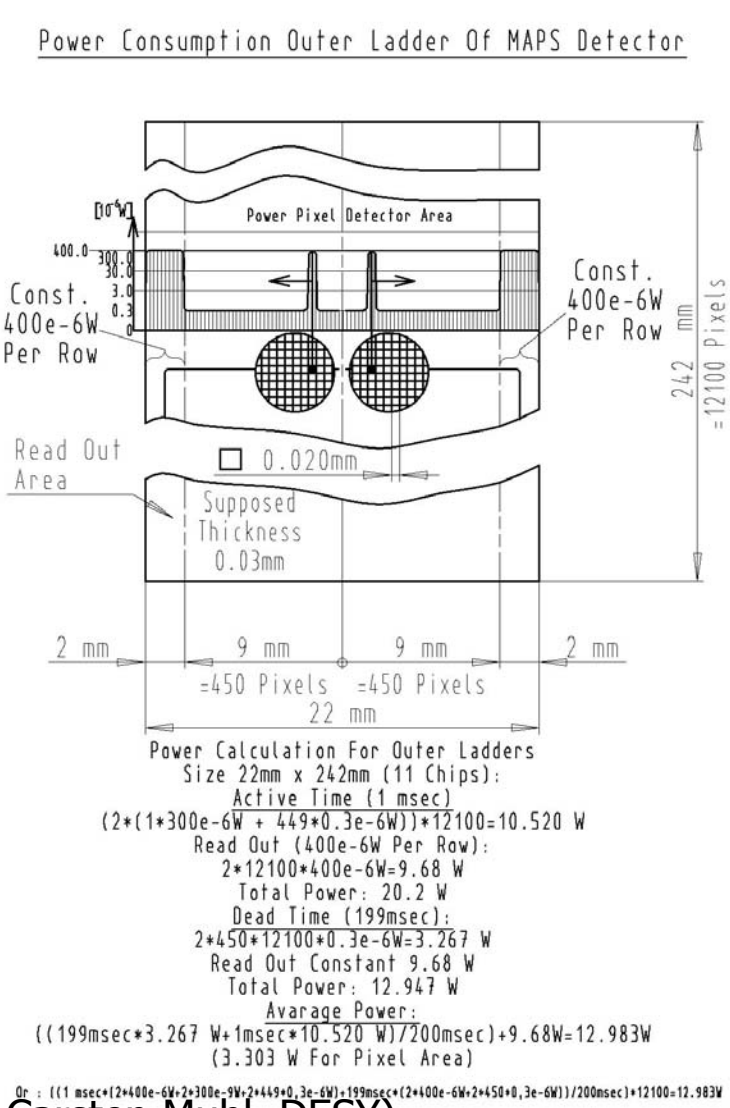
# Power consumption on central ladder (2)



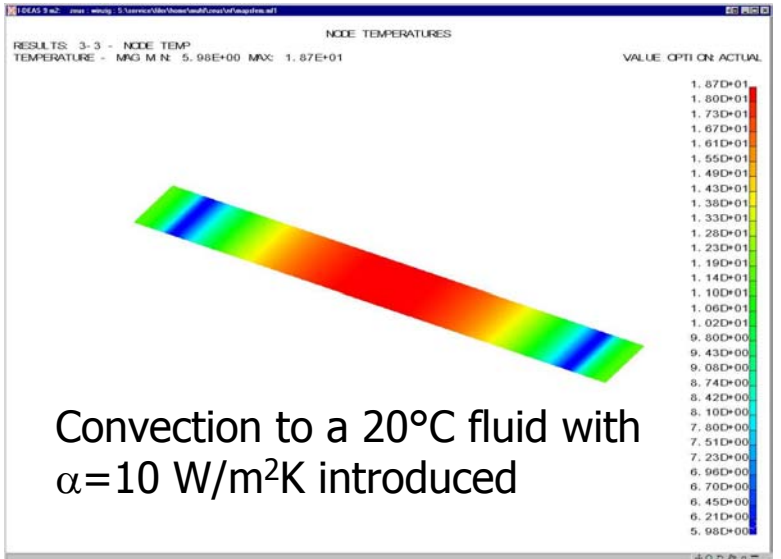




(from Carsten Muhl, DESY)

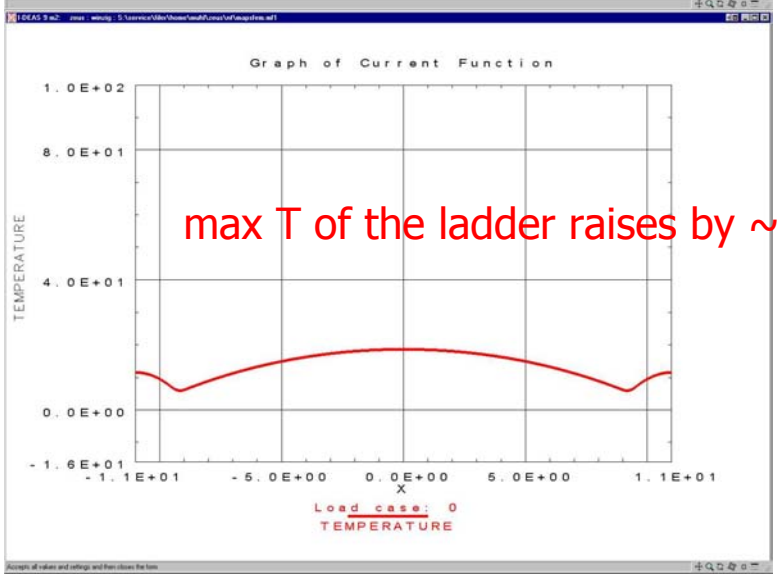
# Power consumption on outer ladder (2)




(from Carsten Muhl, DESY)




Convection to a 20°C fluid with $\alpha$=10 W/m$^2$K introduced




max T of the ladder raises by ~2°C