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Tracking and vertexing opportunities

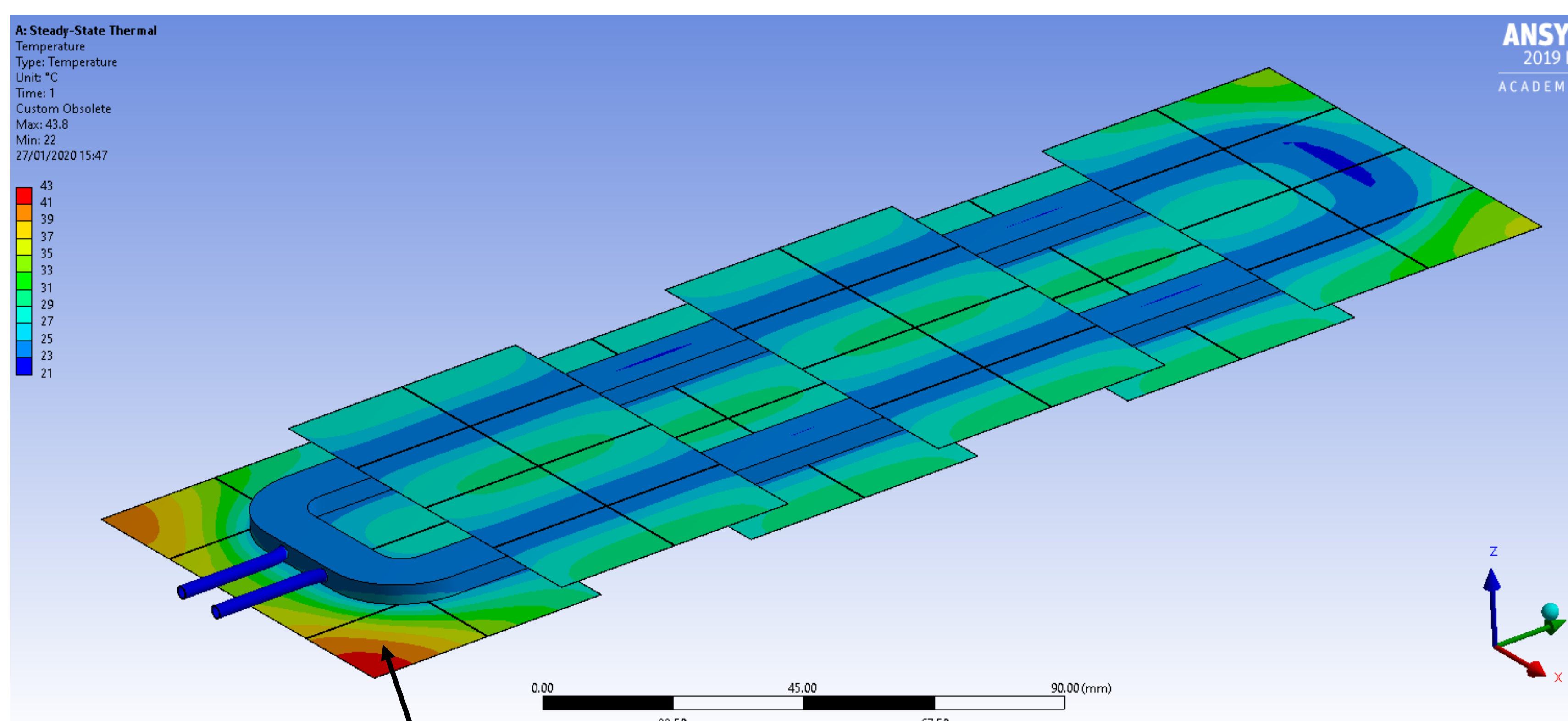
FCC-UK: a discussion concerning UK involvement in the FCC project

Harald Fox (also stand-in for Roy Lemmon)

Thanks to Phil Allport, Laura Gonella, Adrian Bevan, Jaap Velthuis for hints and discussions and to everyone who (unwittingly) contributed slides.

Outline

- Constraints from the accelerator and physics
- Vertexing and tracking in the CLD and IDEA detectors
- Digression into CLIC and ILC
- Sensor technologies
- Power consumption and cooling
- Low mass ultra-thin stitched sensors for vertexing
- ATLASPix as fast tracking sensor
- Low mass detector R&D
- Conclusions



Accelerator and Plan

Table 3.10. Machine parameters.

Parameter	**Z**	**WW**	**ZH**	**$t\bar{t}$1**	**$t\bar{t}$2**
Beam Energy (GeV)	45.6	80	120	175	182.5
Beam current (mA)	1390	147	29	6.4	5.4
Number of bunches	16640	2000	328	59	48
Beam RF voltage (MV)	100	750	2000	9500	10 930
Run time (year)	4	2	3	1	4

Start off with the most challenging condition:

- 20ns bunch spacing
- high number triggers

Table 2.1. Machine parameters of the FCC-ee for different beam energies.

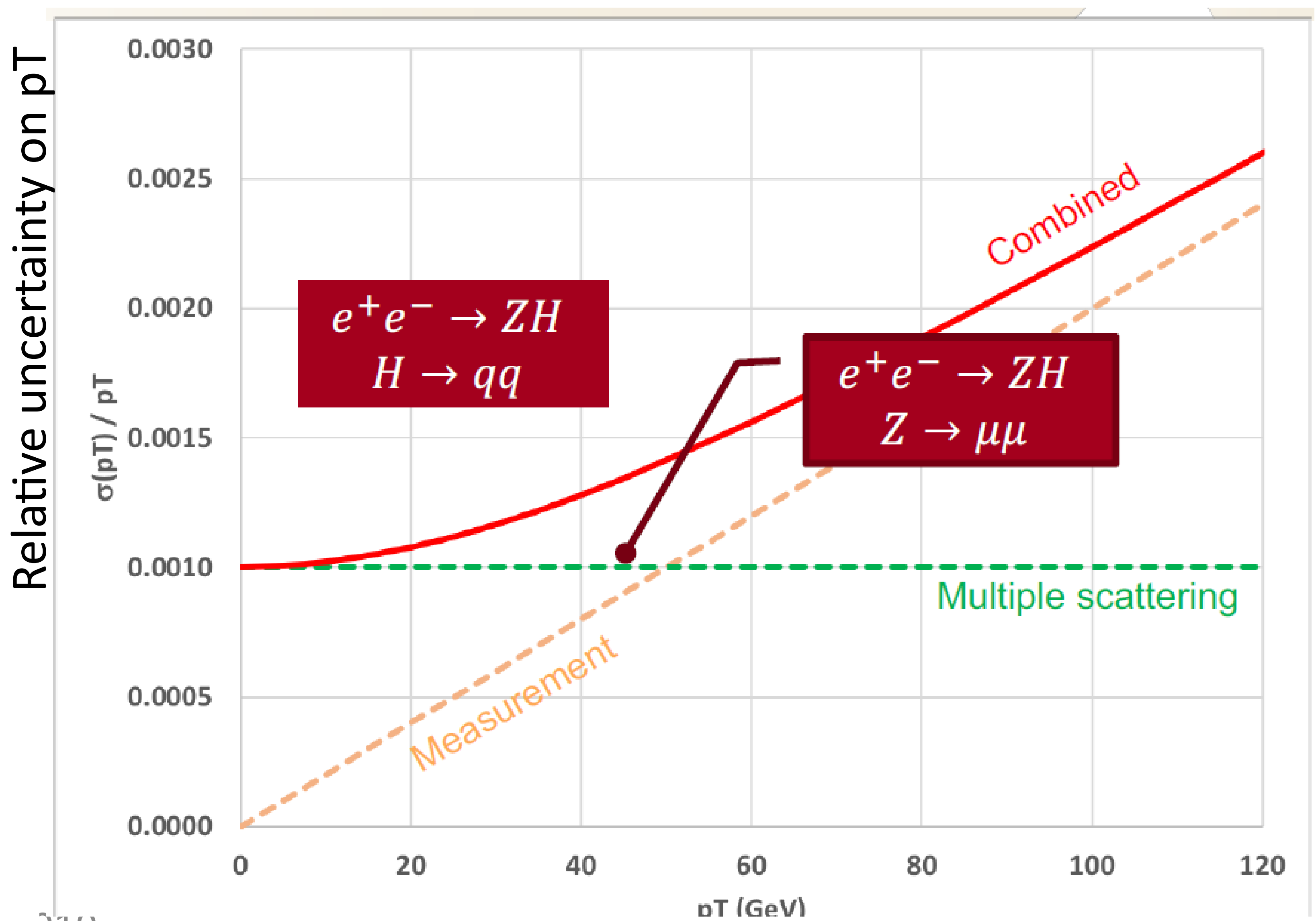
		Z	**WW**	**ZH**	**$t\bar{t}$**	
Circumference	(km)			97.756		
Bending radius	(km)			10.760		
Free length to IP ℓ^*	(m)			2.2		
Solenoid field at IP	(T)			2.0		
Full crossing angle at IP θ	(mrad)			30		
SR power / beam	(MW)			50		
Beam energy	(GeV)	45.6	80	120	175	182.5
Beam current	(mA)	1390	147	29	6.4	5.4
Bunches / beam		16640	2000	328	59	48
Average bunch spacing	(ns)	19.6	163	994	2763[a]	3396[a]

``Low'' field strength requires compensation to achieve good pT resolution

- $\propto L^2$
- $\propto B$
- $\propto \sigma$
- $\propto \sqrt{N}$

pT Resolution

Charlie Young



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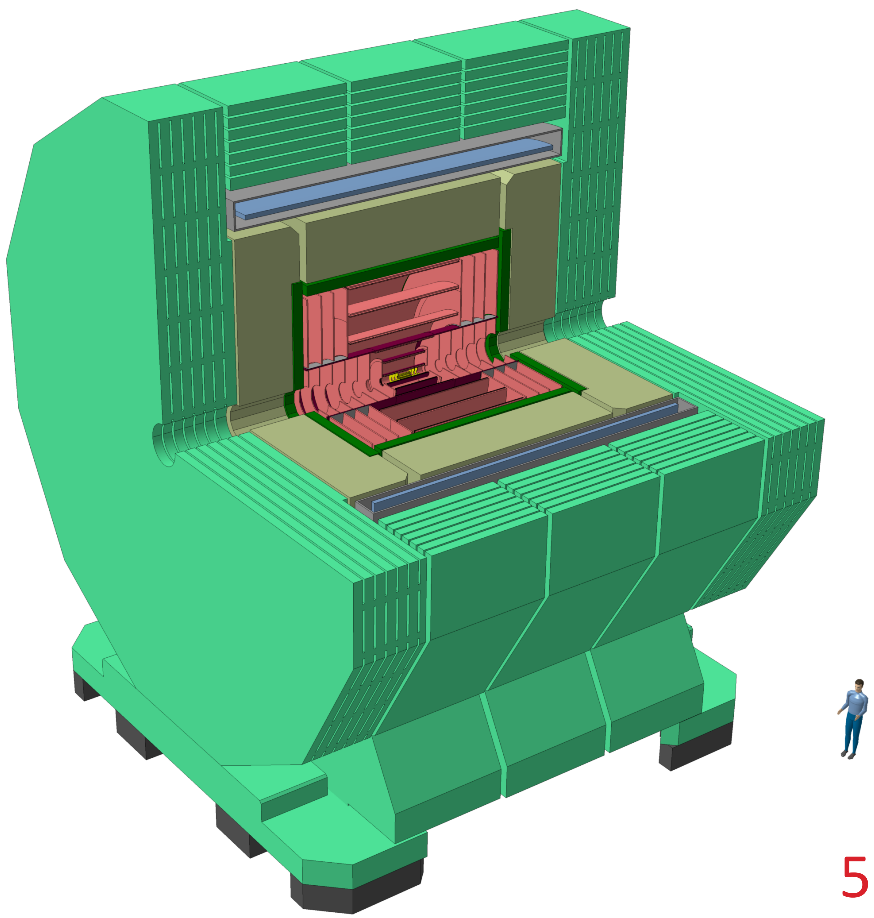
Multiple scattering

$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta}$$

Intrinsic detector resolution

Impact parameter resolution driven by separating b, c, τ

CLD detector



58 m² in outermost layer

<table>
<tr><th>Concept</th><th>CLICdet</th><th>CLD</th></tr>
<tr><td>Vertex inner radius (mm)</td><td>31</td><td>17</td></tr>
<tr><td>Tracker half length (m)</td><td colspan="2">2.2</td></tr>
<tr><td>Tracker outer radius (m)</td><td>1.5</td><td>2.1</td></tr>
<tr><td>ECAL absorber</td><td colspan="2">W</td></tr>
<tr><td>ECAL X_0</td><td colspan="2">22</td></tr>
<tr><td>HCAL absorber</td><td colspan="2">Fe</td></tr>
<tr><td>HCAL λ_I</td><td>7.5</td><td>5.5</td></tr>
<tr><td>Solenoid field (T)</td><td>4</td><td>2</td></tr>
<tr><td>Overall height (m)</td><td>12.9</td><td>12.0</td></tr>
<tr><td>Overall length (m)</td><td>11.4</td><td>10.6</td></tr>
</table>

not (quite) achievable with 180 nm technology

Single point resolution

- 3 double layers 3 × 3 μm for vertex, 0.6% X_0 each
- 5 × 5 μm for innermost disk
- 7 × 90 μm for the rest tracker (25 × 300 μm pixel size); 1-1.5% X0

can be done with large fill factor design

50 / 1100 hits BX in VXD from IPC (Incoherent pair creation) @ 91/365 GeV

- max occupancy 1e-5
- needs to be integrated over a few μs for ``slow'' detectors
- negligible

350 hits/BX from synchrotron rad @ 365 GeV

occupancy O(1e-4

More need for PID?

IDEA detector

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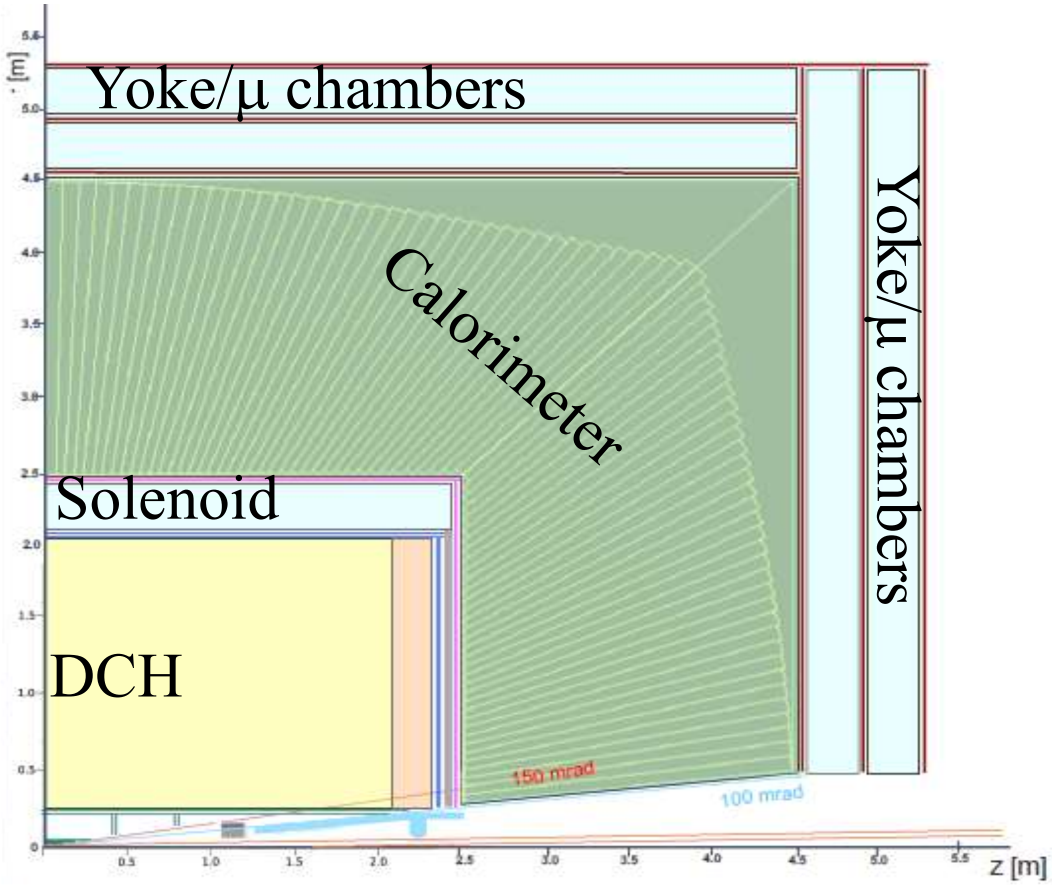
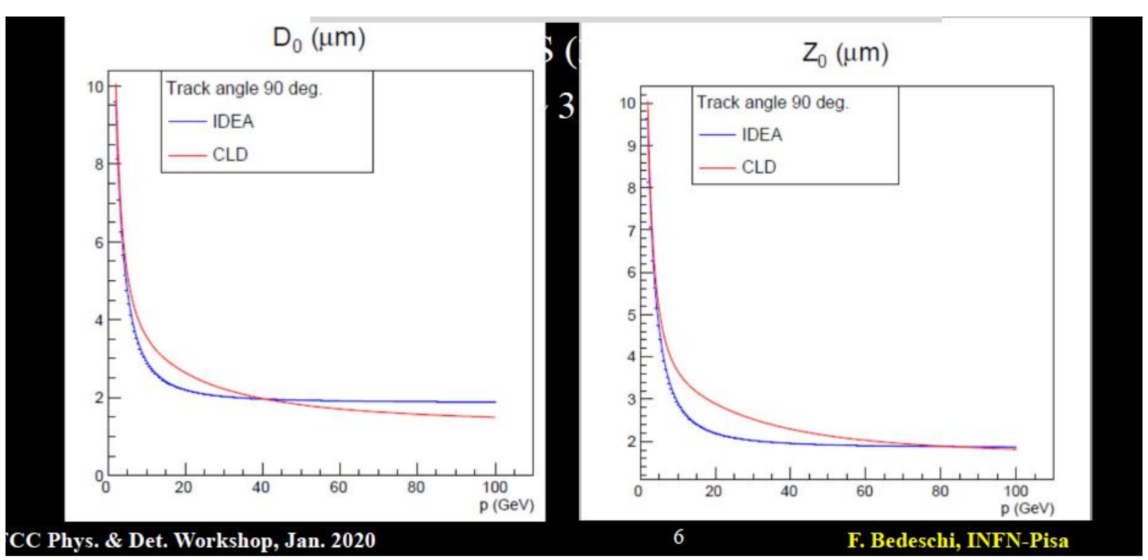
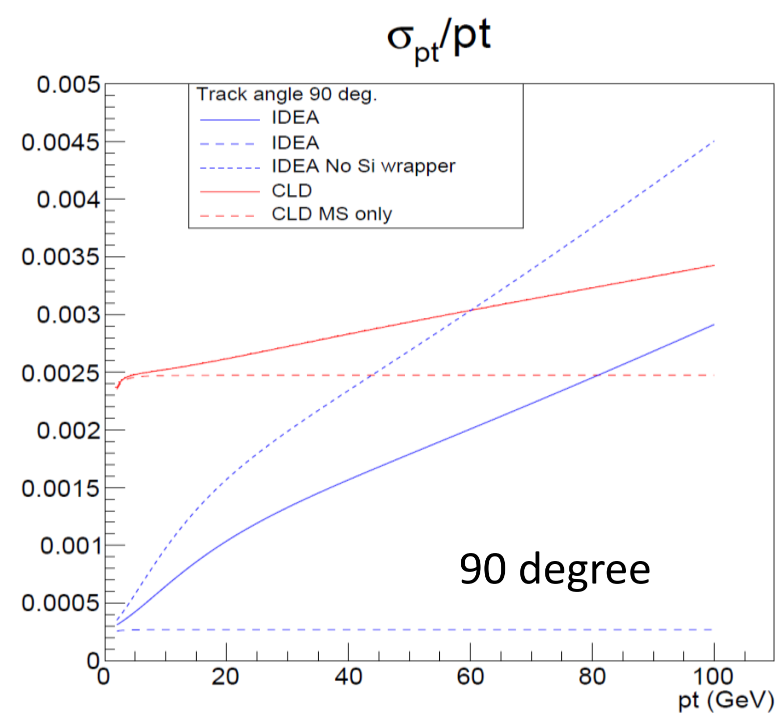


- Vertex detector based on ALPIDE
- 5 × 5 μm point resolution
- 7 layer vertex system @ 0.3% X_0 per layer



- Outer vertex layer at r = 34cm
- Fast drift chamber
- 1.6% X_0 in total
- DCH also provides good PID
- 2 layer Si wrapper at r ≈ 2m



Large # of measurement points and lower X/X_0 of DC + wrapper winning over better hit resolution of Silicon

D. Contardo, FCC Week, January 2020

Digression into CLIC and ILC

Linear

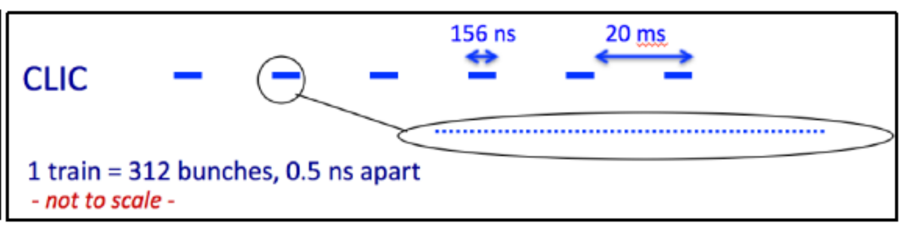
Parameter	250 GeV (ILC)	500 GeV (ILC)	380 GeV (CLIC)	1.5 TeV (CLIC)	3 TeV (CLIC)
Luminosity L ($10^{34}cm^{-2}sec^{-1}$)	**1.35**	**1.8**	**1.5**	**3.7**	**5.9**
L > 99% of √s ($10^{34}cm^{-2}sec^{-1}$)	1.0	1.0	0.9	1.4	2.0
Repetition frequency (Hz)	5	5	50	50	50
Bunch separation (ns)	554	554	0.5	0.5	0.5
Number of bunches per train	1312	1312	352	312	312
Beam size at IP σ_x/σ_y (nm)	515/7.7	474/5.9	150/2.9	~60/1.5	~40/1
Beam size at IP σ_z (μm)	300	300	70	44	44

ILC: Crossing angle 14 mrad, e^- polarization ±80%, e^+ polarization ±30%
CLIC: Crossing angle 20 mrad, e^- polarization ±80%

Very small beams + high energy => beamstrahlung

Very small bunch separation at CLIC drives timing requirements for detector

Very low duty cycle at ILC/CLIC allows for:
Triggerless readout
Power pulsing



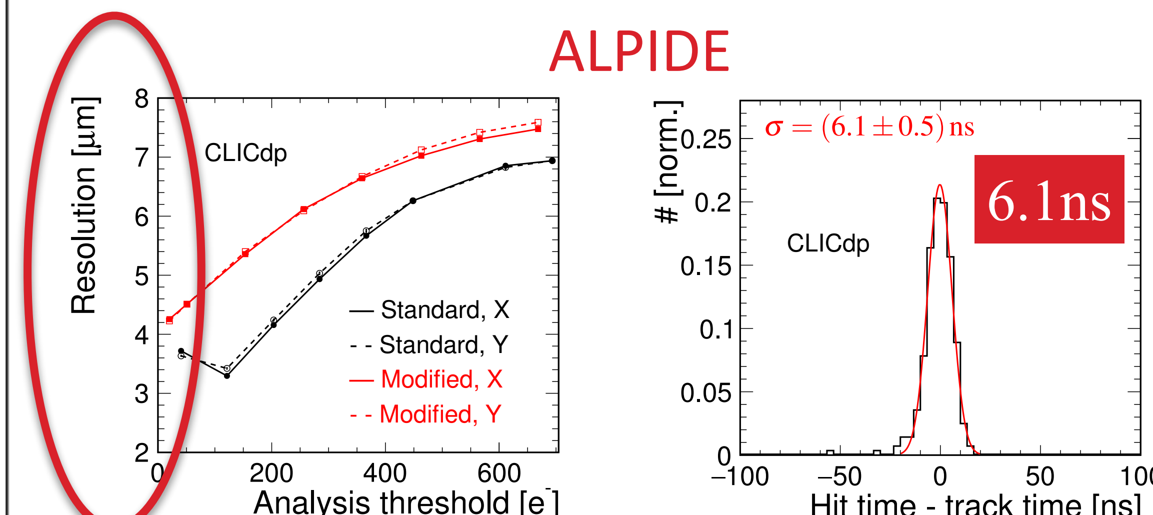
Bunch trains with long periods of no interaction ⇒ Power pulsing

- Reduces average power
- Reduces cooling needs
- Lower X_0 (× 1.5 in FCC CDR)

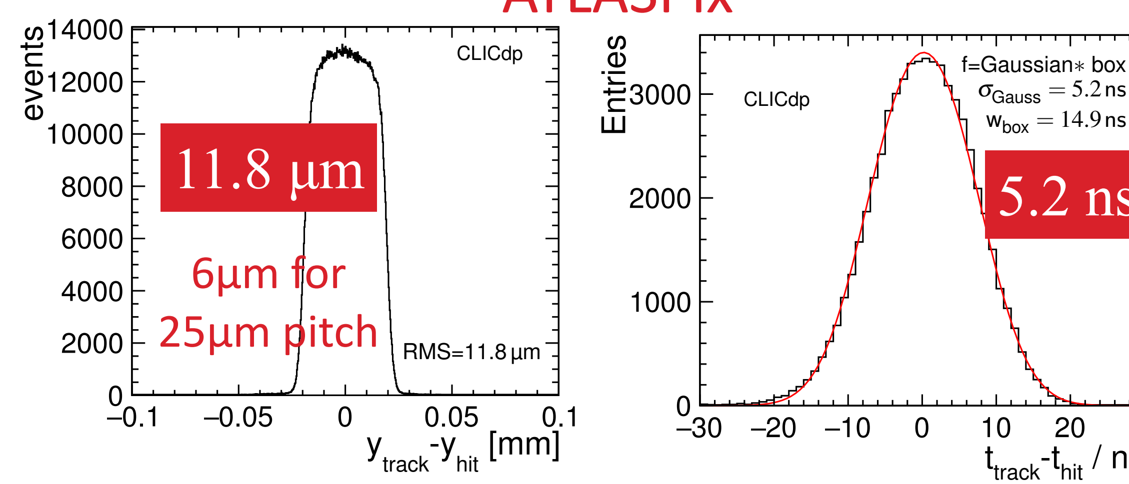
See e.g. *A. Besson, FCC-ee workshop, January 2020* for an example calculation based on MIMOSIS-I

CLIC comprehensively investigated sensor options: *Yellow Report, Detector Technologies, 2019*

ALPIDE



ATLASPix



Power pulsing at linear colliders

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MIMOSIS-1 = ALPIDE + high rate capability

ILC Power: Results

- Chip read-out speed
  - 2 μs - 4 μs
- Power pulsing
  - Power ON, no beam during 1-3 ms
    - Leading parameter With NO P.P.
  - Power OFF: 10-30 mW/chip
    - Leading parameter with P.P.
- Outer layers
  - Lower occupancy, larger surface
  - Power is dominated by outer layers
- Beam background rate
  - TDR – TDR × 2
- Resolution

Power Analog ($mW/chip$)	49.22
Power Bias ($mW/chip$)	4.5
Power PriorityEncoder ($mW/chip$)	4.219
Power DigitalPeriphery ($mW/chip$)	64.27
Power PLL ($mW/chip$)	18.5
Power Serializer With Data ($mW/chip$)	86.06
Power Serializer With No Data ($mW/chip$)	0
Power LVDS ($mW/chip$)	56.4

Period	Relative Energy
E during train	225 mJ ~ 4 %
E between train (Power ON)	380 mJ ~ 6 %
E between train (Power OFF)	5740 mJ ~ 90 %

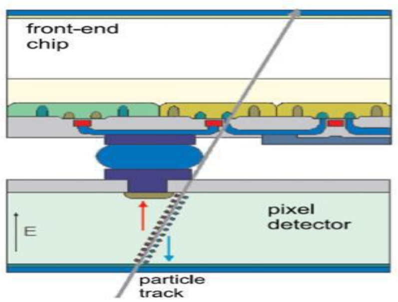
Layers	Relative Power
Layers 0/1	~ 10 %
Layers 2/3	~ 35%
Layers 4/5	~ 55 %

Pitch	Resolution	Power
30 μm	~ 5 μm	1
22 μm	~ 4 μm	×2 (matrix)
18 μm	~ 3 μm	×4 (matrix)

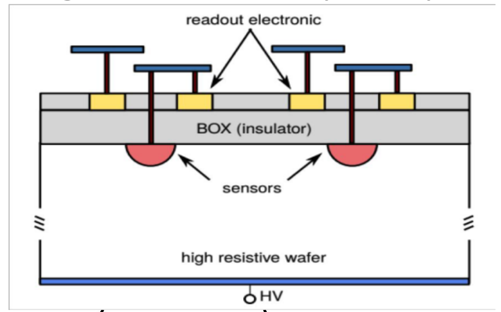
Beam background	Read-out speed	<Power (NO P.P.)	<Power> (P.P.)	
rate	(μs)	(W)	Conservative	Ambitious
TDR	4 μs	102 W	~31 W	~12 W
TDR	2 μs	122 W		
TDR x 2	4 μs	107 W		
TDR x 2	2 μs	127 W		

Some recent Silicon technology demonstrators ($\simeq$ 2 x 2 cm^2)

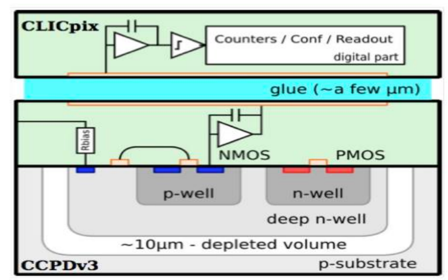
Smaller pitch and thinner planar and 3D sensors for resolution



SoI process Si/ASIC wafers connected through Insulator Oxyde layer



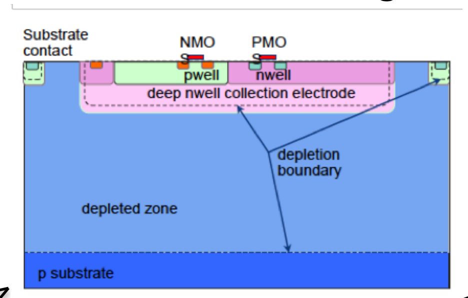
Capacitive Coupling of HV CMOS design to ASIC through insulating glue

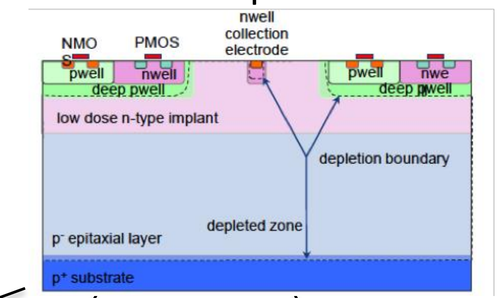


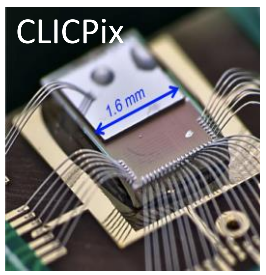
Modified HV-CMOS depletion (< 100 V)

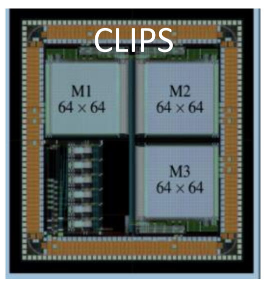
Modified HR-CMOS depletion (6V)

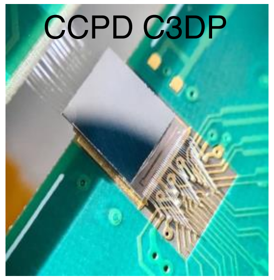
with faster and higher rate readout capabilities

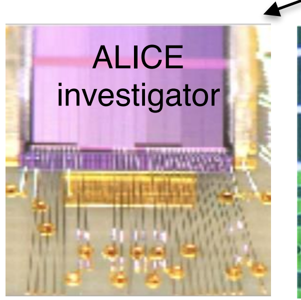


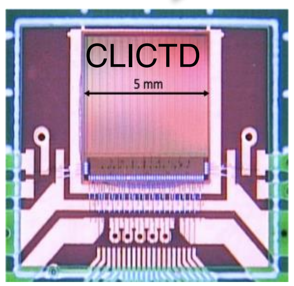


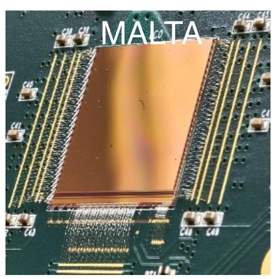












Silicon sensor R&D	Hybrid	SoI			CMOS Monolthitic			CCPD	CMOS
Demonstrator	CLICpix	Cracov	CLIPS (CLIC)	ALICE investigator	CLICTD	Malta/Monopix	ATLASpix(Mu3ePix)	C3DP+CLICpix	ITS3
Sensor	planar	planar	planar	HR-CMOS standard	HR-CMOS modified process		HV-CMOS		HR-CMOS
Connection to readout electronics	bump bonding	SoI	SoI	momolithic	monolthitic	monolithic	monolitic	CC with glue	monol
ASIC technology (nm)	65	200	200	180(TJ)	180 (TJ)	180(TJ)/150(LF)	180(AMS)/150(LF)	65	65(TJ)
Thickness (µm)	50 / 200	300 / 500	100 / 500	100	50 / 100	100	60	50	20-40
Pitch/cell size (µm x µm)	25 x 25	30 x 30	20 x 20	28 x 28	30 x 300	36 x 36	40 x 130	25 x 25	20×20
Hit resolution (µm)	9 / 3.5	5/2		4		4	12	7	
Time resolution (ns)				6		< 10	5	7	2
Max NIEL (1 MeV neq/cm2)/TID (Mrad)	O(10^{16})/Grad			O(10^{15})/300			O(10^{15})/100		

ATLASPix3:
50 × 150 µm
can be
25 × 300 µm

D. Contardo, FCC Week, January 2020

Power consumption

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	Readout speed	Analog Power mW/cm²	Digital Power mW/cm2	Serial Powering
Mimosa28	185.6 μs 160 MHz	41+63	46 20 cm	
Alpide	50/200 kHz 400Mbps	6 (in matrix)	34 1.5 cm	
Malta	25 ns	70	3 - 80	
AtlasPix3	25 ns 400 Mbps	30	110 50 cm	
ITS3 65nm		<20 (pixel matrix)	34 × 4 ? 28 cm	

STAR was able to air-cool Mimosa28, without disks (sic!).
All sensor options are within a small factor of each other
Can we save power by slowing the sensor down, or being clever with a data aggregator?

Stitching and power consumption

- ALPIDE power consumption in the matrix:
  - Analog ~ 5 mW/cm^2
  - Digital ~ 1 mW/cm^2

Sensitive area: 4.12 cm^2
Inner Barrel: 36.9 mW/cm^2
Outer Barrel: 20.2 mW/cm^2
In the matrix:
(analog + digital)/area
$(22.2 + 3.2)/4.12 = 6.2$ mW/cm^2

- Analog will hopefully not increase too much, but digital will if we are not careful
- Data will be transmitted over 28 cm instead of 1.5 cm so 20x in distance, digital power density will increase with the same factor if line toggles are not reduced… (example see next slide)

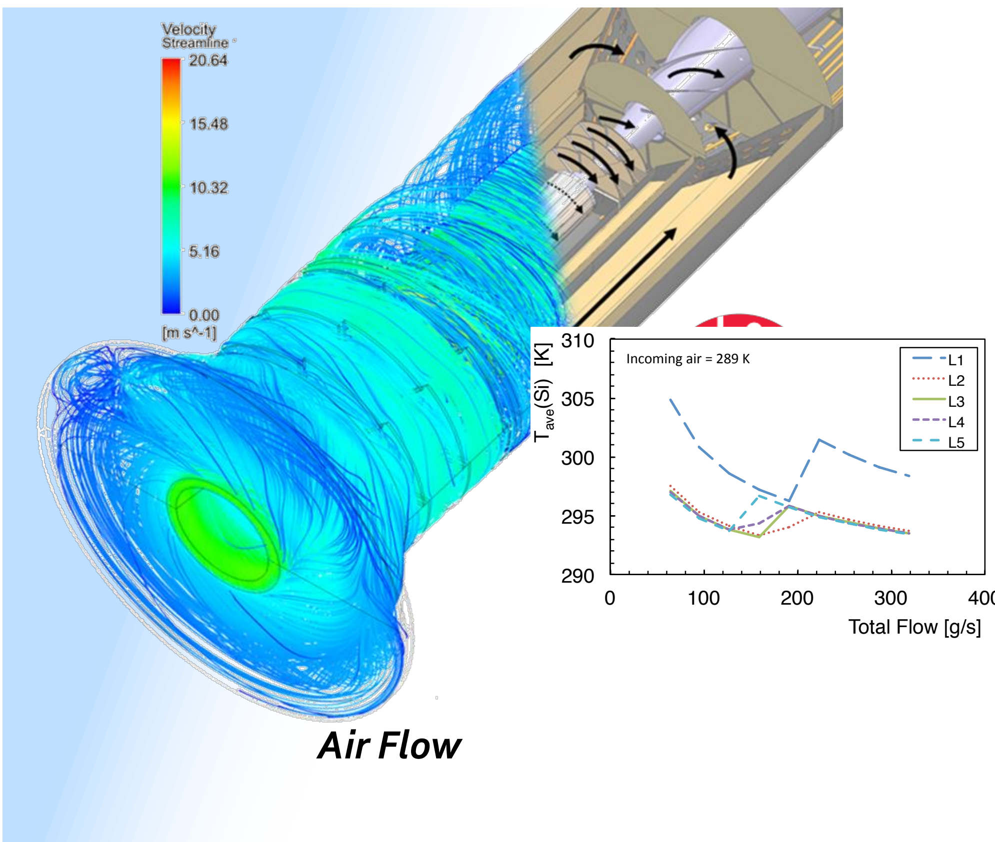
walter.snoeys@cern.ch

There is a factor of 4-5 possible in reduction

W. Snoeyes, FCC Workshop, January 2020

Cooling I

Air cooling



The **STAR** detector cools 2 layers of MIMOSA28 sensors (150mW/cm²) with an air flow of 10 m/s, but **without disks**.

CLIC studied 50mW/cm² for the CDR.

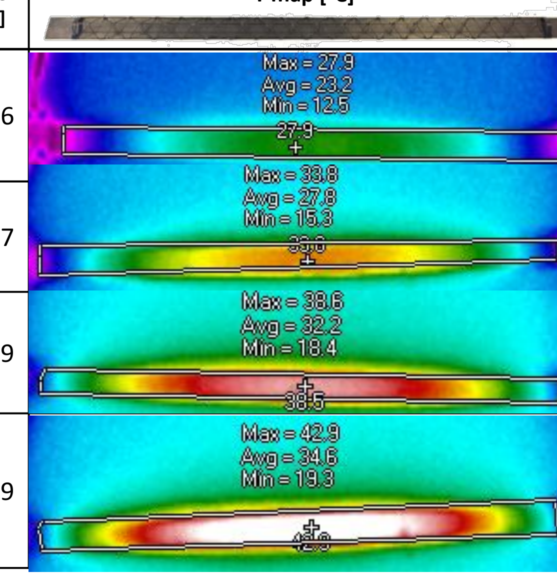
UK experience with **Mu3e** and **PLUME**.

End-of-stave cooling

ALICE investigated end of stave cooling for their upgrade.

Roughly **half of the input power can be absorbed,** leaving a **ΔT** of up to **23℃** within the stave.

q [W cm⁻²]	Power input [W]	Estim. power to flow [W]	T water [°C]	T map [°C]
0.02	0.82	0.56	12.6	
0.03	1.25	0.71	12.7	
0.04	1.64	0.80	12.9	
0.05	2.02	0.86	12.9	



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Water leakless (<1bar) baseline

Water in 15°C--->Tchip <30°C

Pixel max temperature non-uniformity < 5°C

Pressure drop ΔP below 0.3 bar

q [W cm⁻²]	G [L h⁻¹]	$\Delta T_{CHIP-H2O}$ [K]	ΔT_{H2O} [K]	Δp [bar]	$\Delta T_{HEATERS}$ [K]	v_{H2O} [m s⁻¹]
0.15	6.3	6.7	6.9	0.08	4	0.31

G. Gargiulo, CLIC Tracker Technology Meeting, 28/5/15

Cooling II

ATLAS uses **evaporative CO2 cooling** within thin Ti pipes running within the staves.

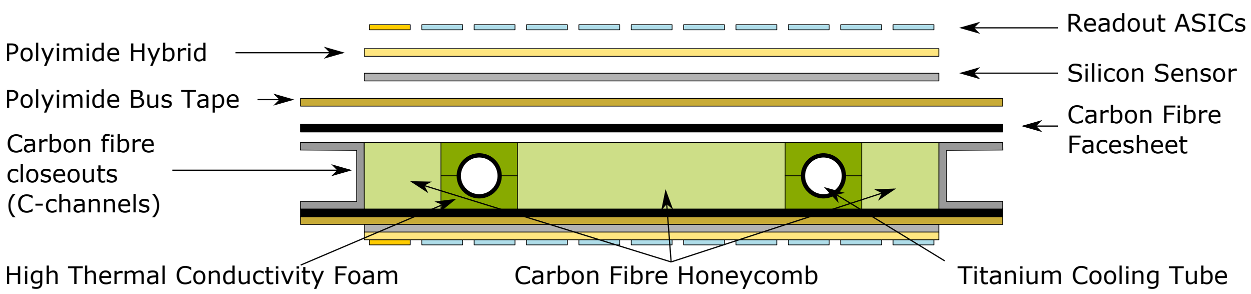


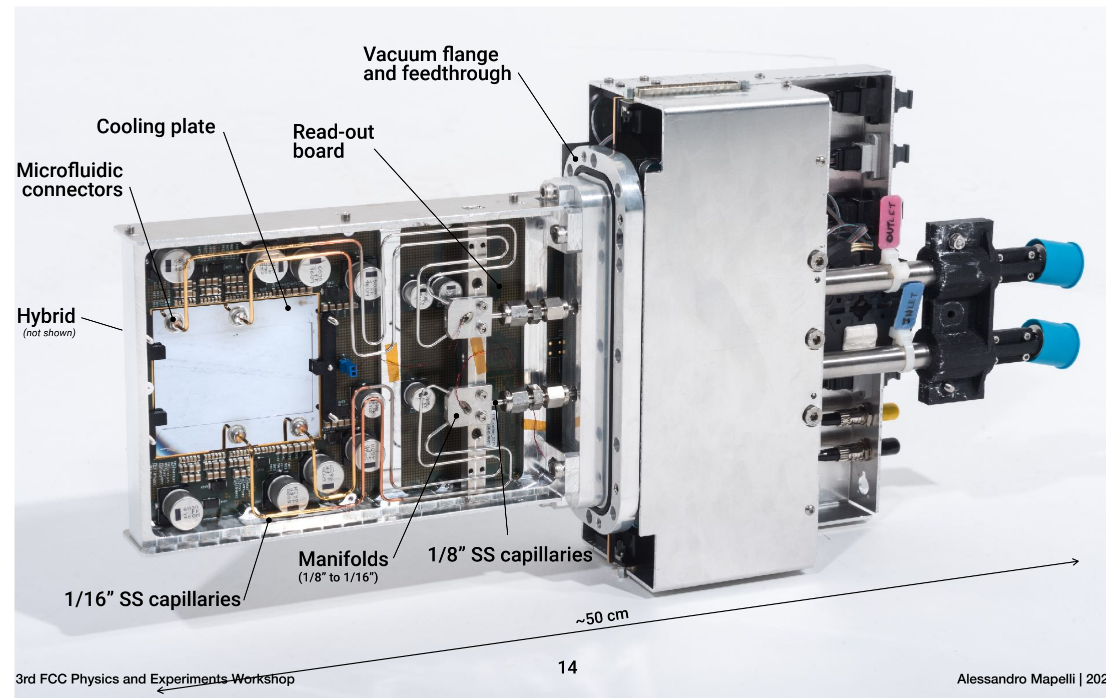
Figure 9.1: Schematic of the internal structure of the stave core, with the silicon sensors and ASICs added. Glue layers are not shown. Not to scale.

Technology of bending and welding of thin-walled Ti pipes has been developed over the **last decade in the UK**.

CO_2 cooling is very powerful.

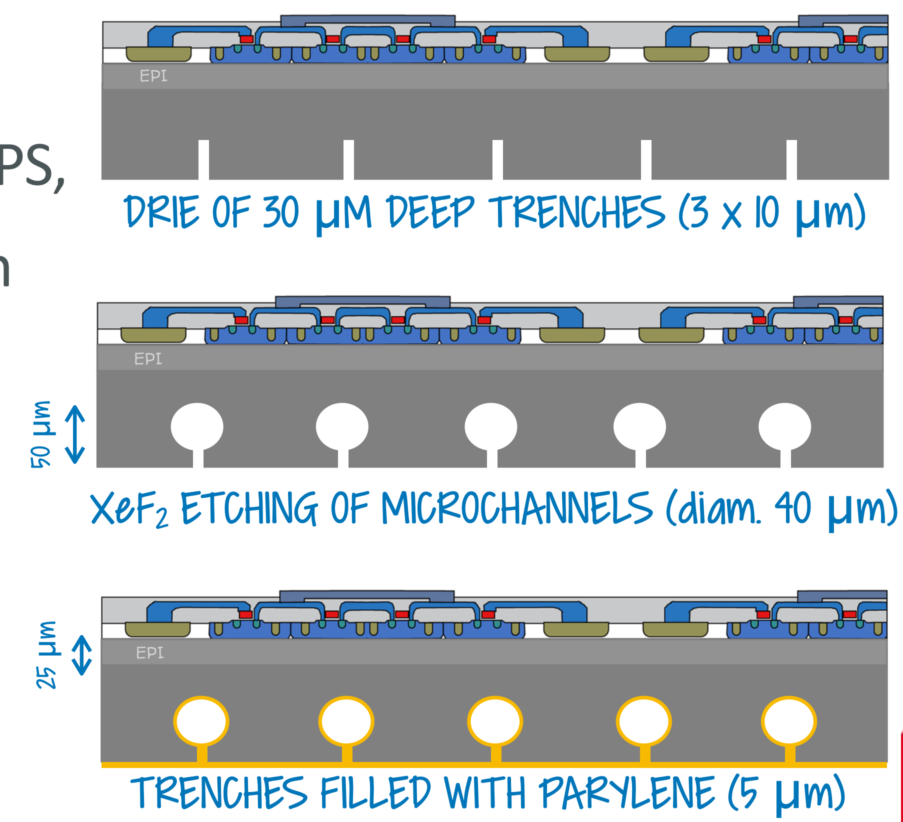
Other evaporative coolants (e.g. C_4F_{10}) are possible.

ALICE, LHCb and NA62 develop **micro-channel cooling**



For use is CMOS MAPS,

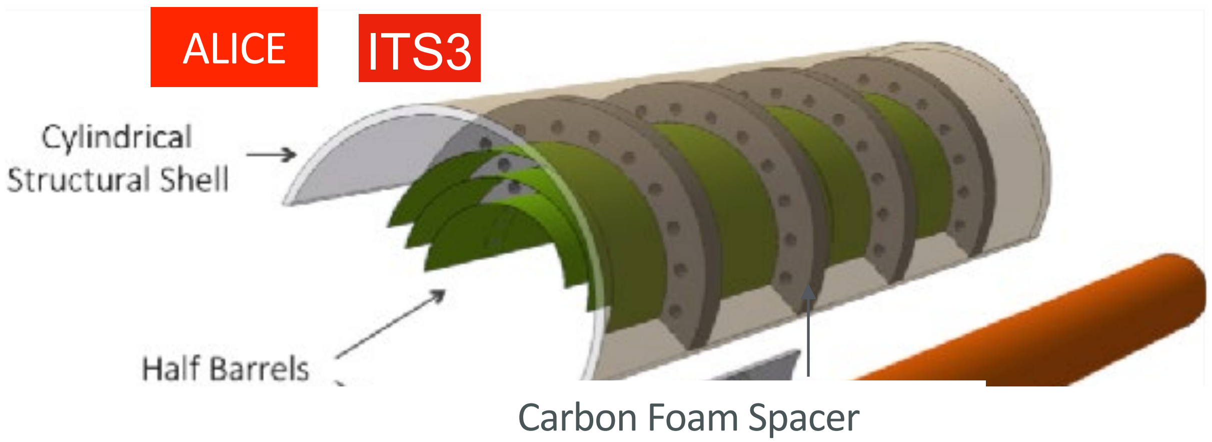
e.g. BCTs in MALTA

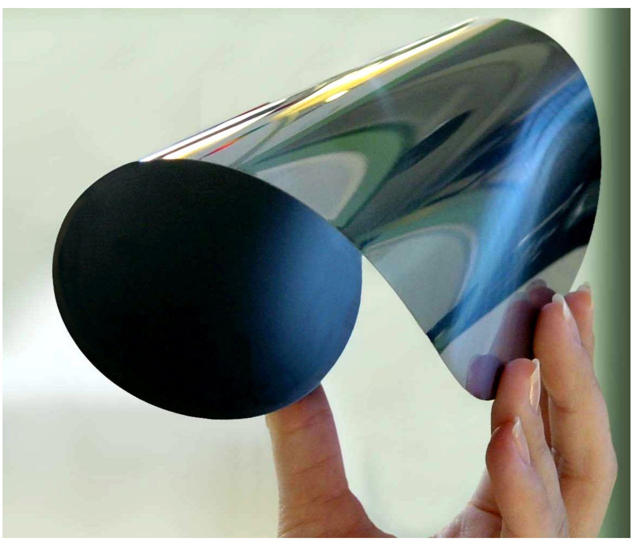


Work in the UK…

A. Mapelli, 3rd FCC Physics and Experiments Workshop 13-17 January 2020 indico.cern.ch/event/838435

TowerJazz Ultra Thin 65nm Sensor





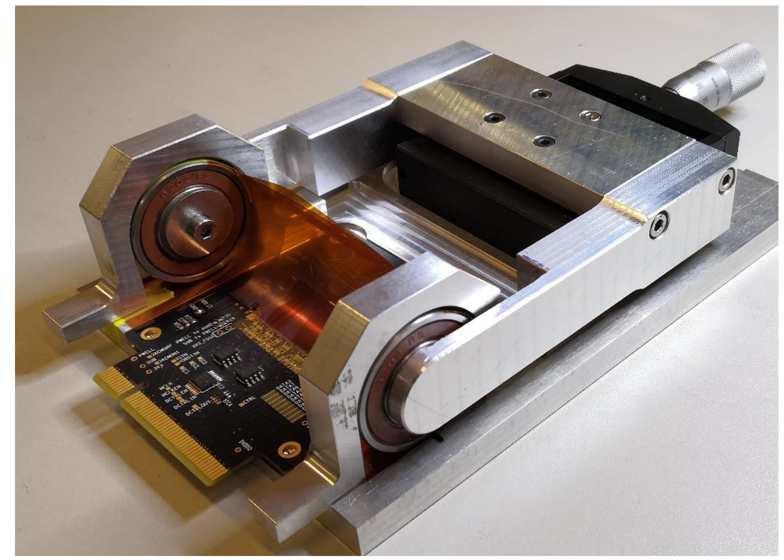
based on:
- wafer-scale (up to ~28x10 cm),
- ultra-thin (20-40 µm),
- bent (R=18, 24, 30 mm)

Si sensors (MAPS)

Aim: 0.3% → ~0.03% X0

65nm technology is mainly for going to 8” wafers!

- **Bent along the short side**
  - Bending affects pixel matrix only
  - Bonding area is glued: flat and secured
  - Variable curvature (down to 1 cm radius)



(Thinned Alpide sensor)

Pixel pitch O(10µm): **20 × 20 µm**

Shorten integration time 5µs → 2µs

Participating institutes: LBNL, Birmingham, RAL CMOS Sensor Design group, Wuhan, BNL instrumentation division, JLAB, Daresbury and Liverpool, plus many interested institutes

Development driven by **ALICE (and EIC)**, but clearly of interest for Higgs factories!

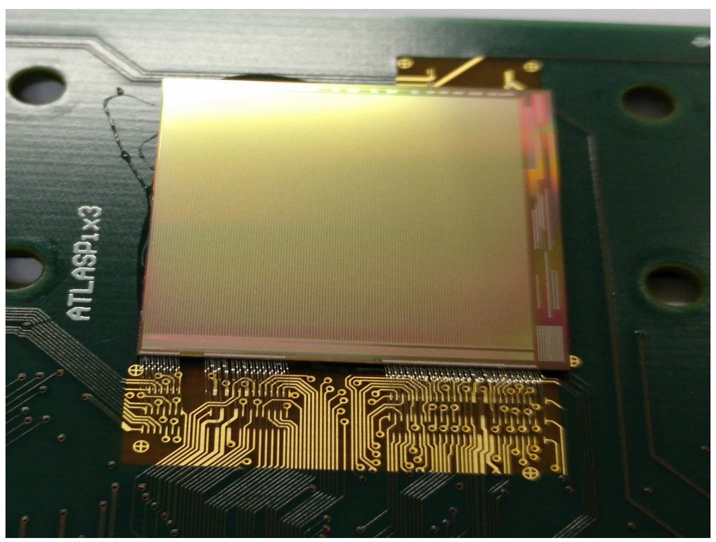
G. Contin and L. Gonella, 2020 EIC SVT Workshop

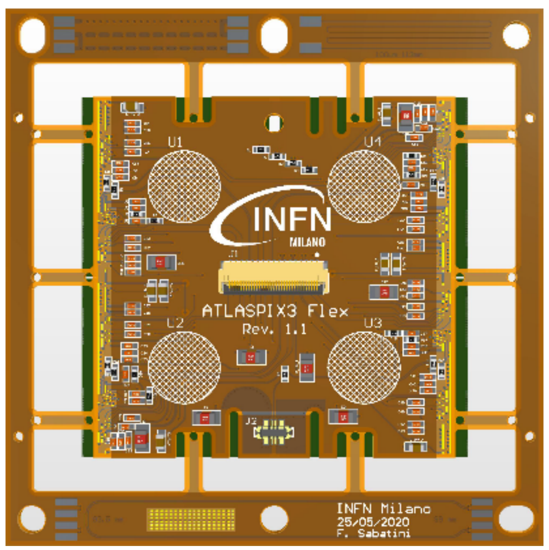
ATLASPix3 for tracking

Full size (2 × 2 cm sensor) designed for LHC

Fully functional: successful test beam at DESY

Sizable community developing: Bristol, Edinburgh, Lancaster, Liverpool and RAL; Daresbury, Oxford, QMUL, Sheffield and Warwick; Karlsruhe; Como, Milano, Pisa and Torino; several Chinese groups

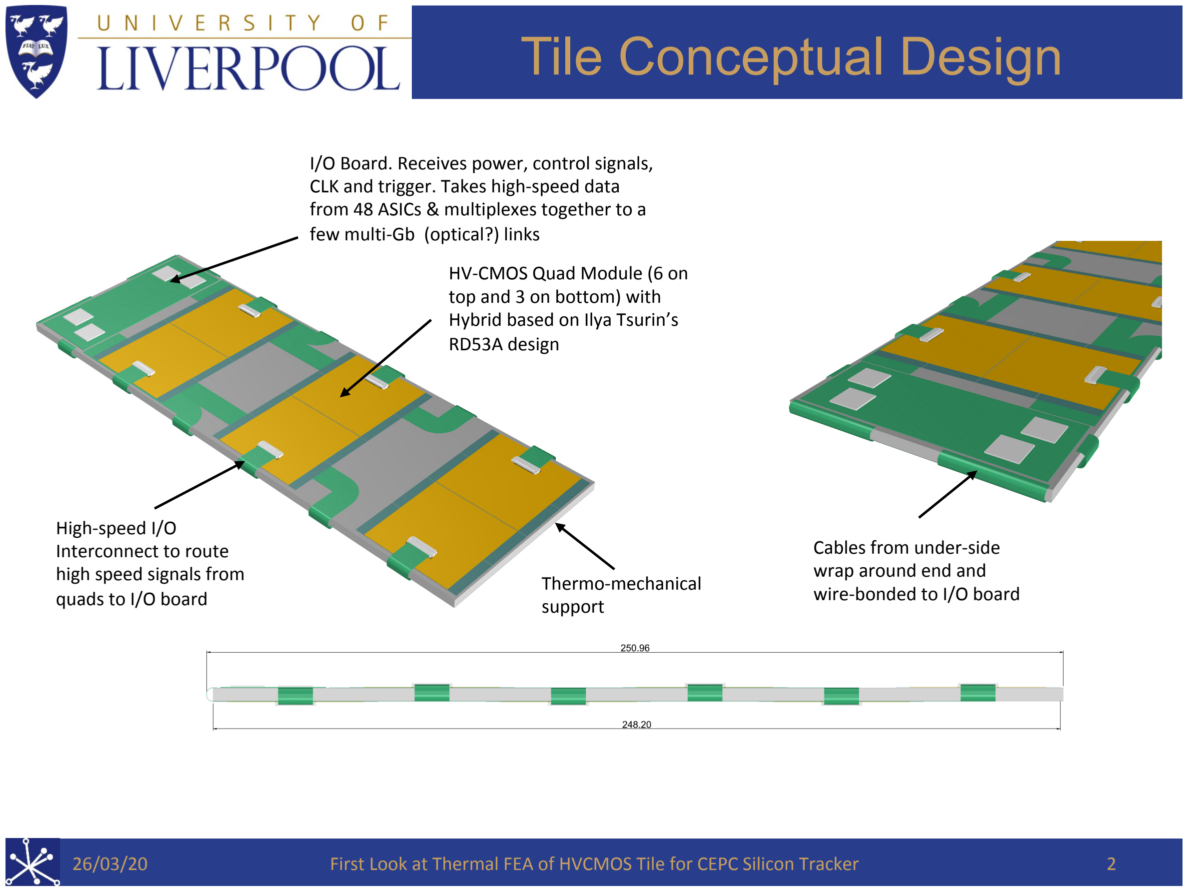




Eva Vilella-Figueras part of the design team. Close relations to MuPix for the **Mu3e experiment**

A candidate sensor for the **LHCb Mighty Tracker** upgrade.

Single chip boards to be bonded and distributed to participating institutes



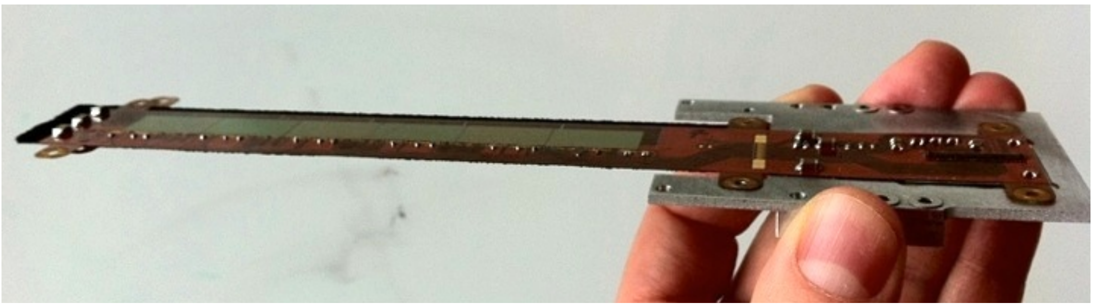
Test evolvement of ATLASPix3 (MPW submission):

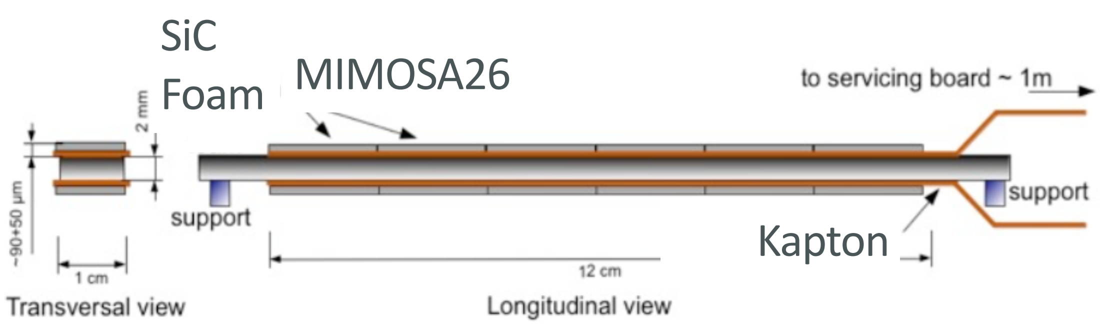
- Smaller pixel size (**25μm**) in ϕ direction
- **Lower capacitance**
- **Amplifier and comparator design**
- Electronics in **pixel or periphery**
- **Data aggregation** between chips

Other UK Activities

Physics Lancaster University

PLUME (Bristol, Strsbourg, DESY, Frankfurt)

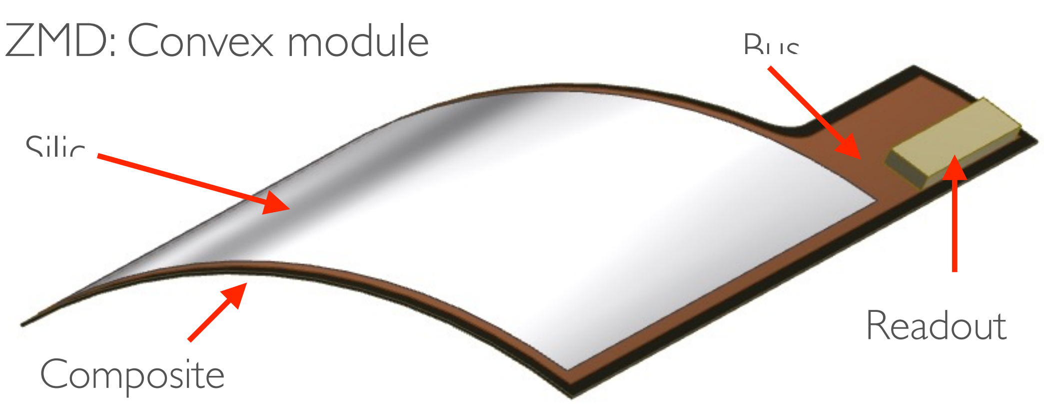




0.35% X_0 towards ~0.1% X_0

J. Goldstein, 2019 CEPC Workshop, Oxford

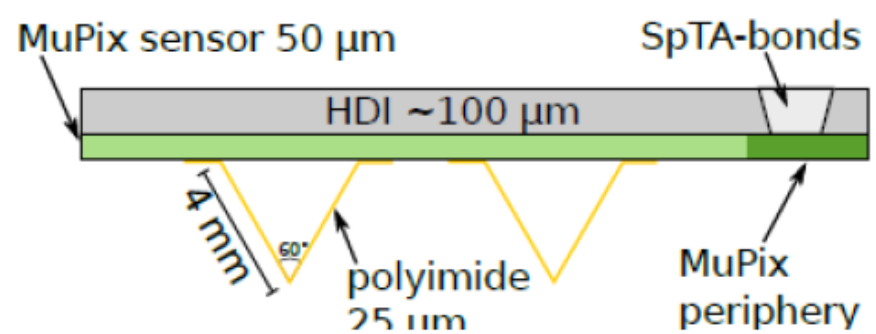
ZMD (QMUL, RAL & Micron)



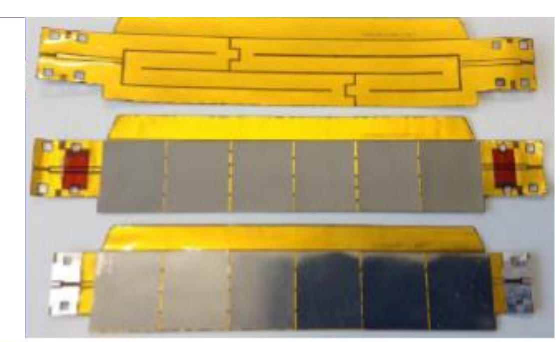
Mu3e (UK: Bristol, Liverpool, Oxford, UCL)

Perspective

Experiment	Ref.	x/X_0 per layer [%]
ATLAS IBL	[1]	1.9
CMS Phase I	[2]	1.1
ALICE upgrade	[3]	0.3
STAR	[4]	0.4
Belle-II IBL	[5]	0.2
Mu3e		**0.1**



Lay-up of MuPix ladder, with v-channels

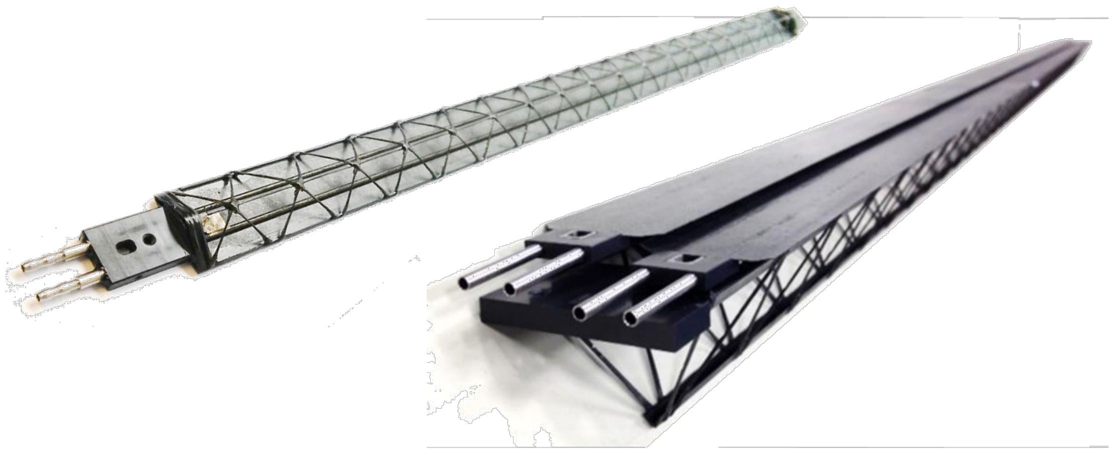


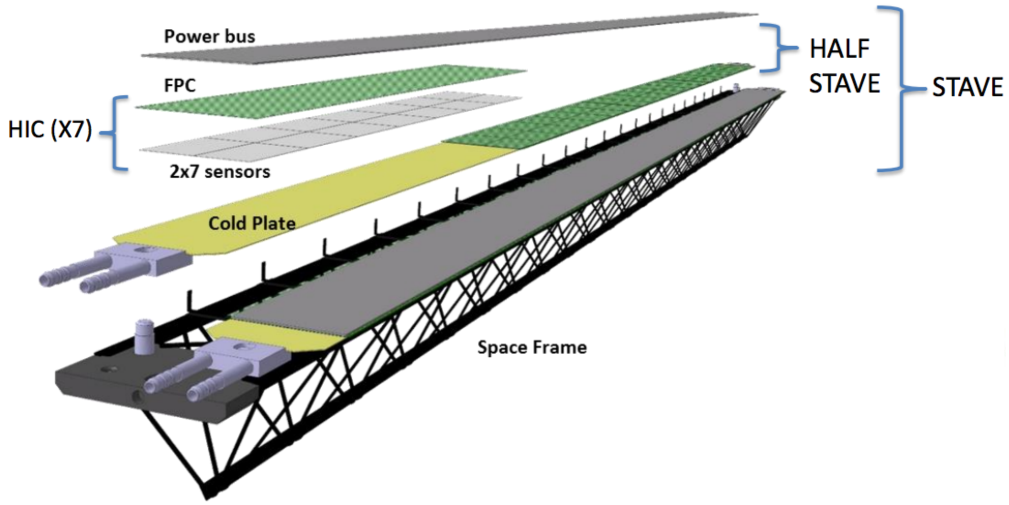
I Bare flex
II with spacer and steel chips.
III ends folded over

K. Arndt, 2019 CEPC Workshop, Oxford

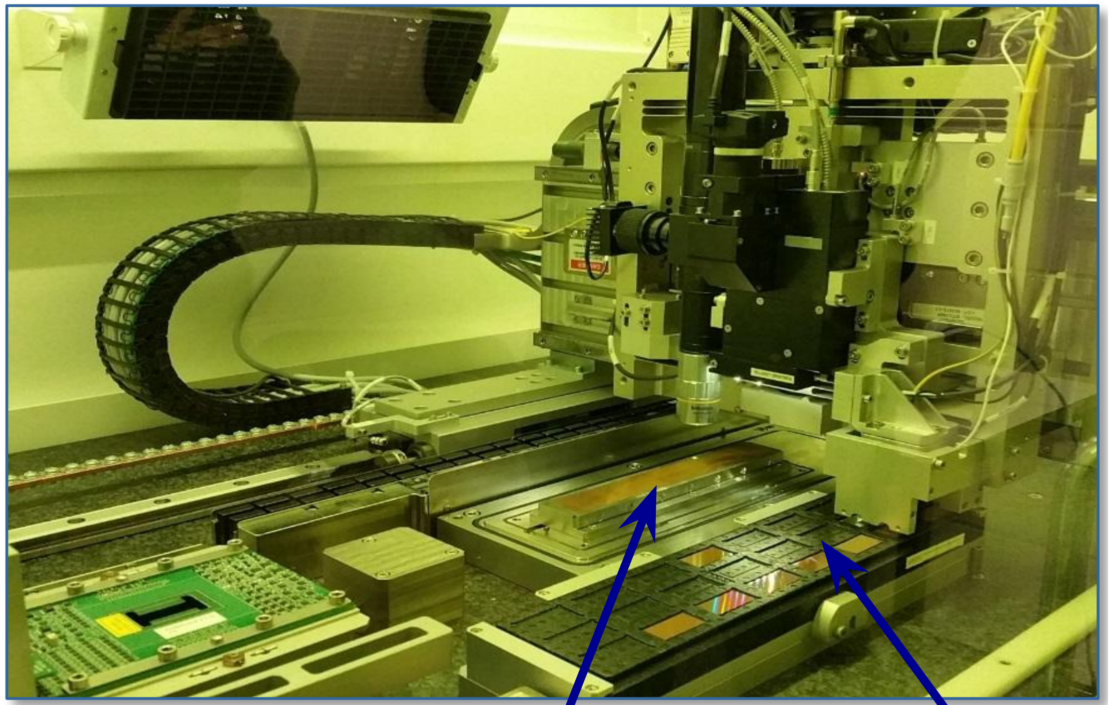
Support structure: ALICE

Physics Lancaster University

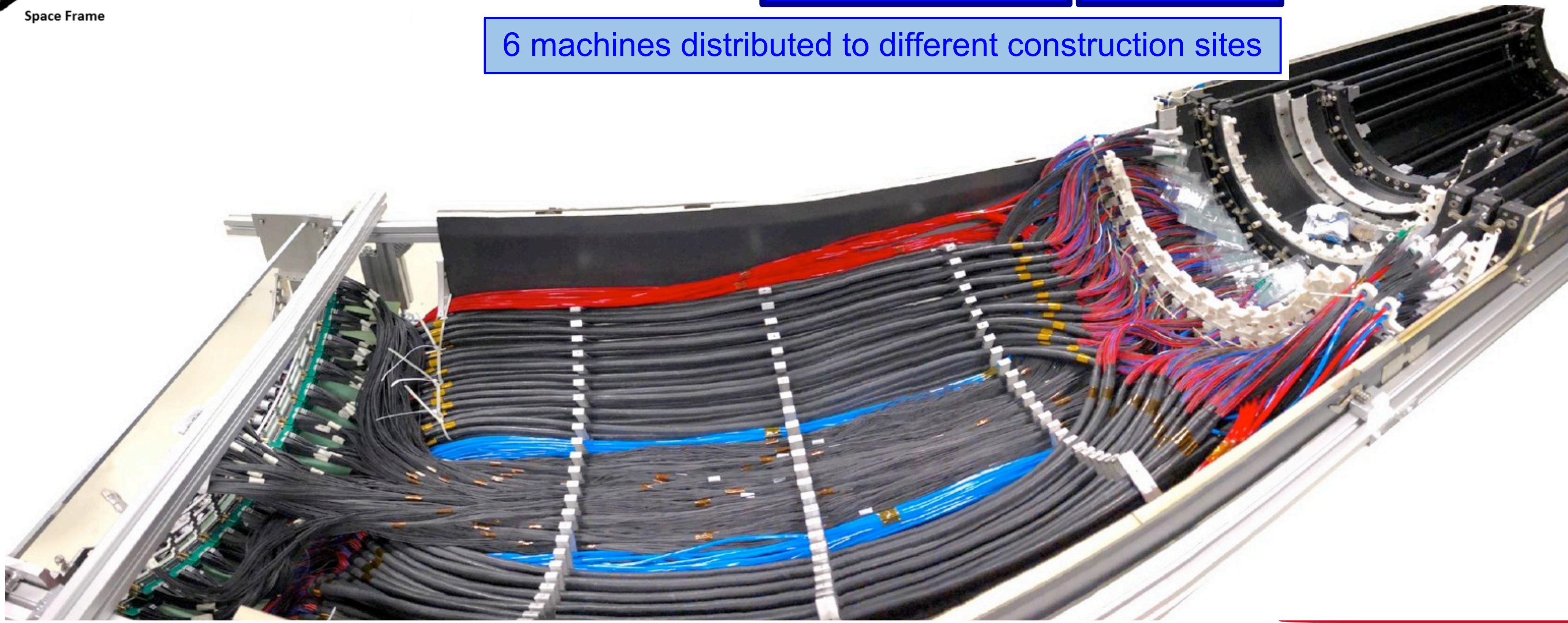




Infrastructure in Liverpool & Daresbury



6 machines distributed to different construction sites



H. Fox

Stave: ATLAS Pixel Carbon Fibre Support Structure

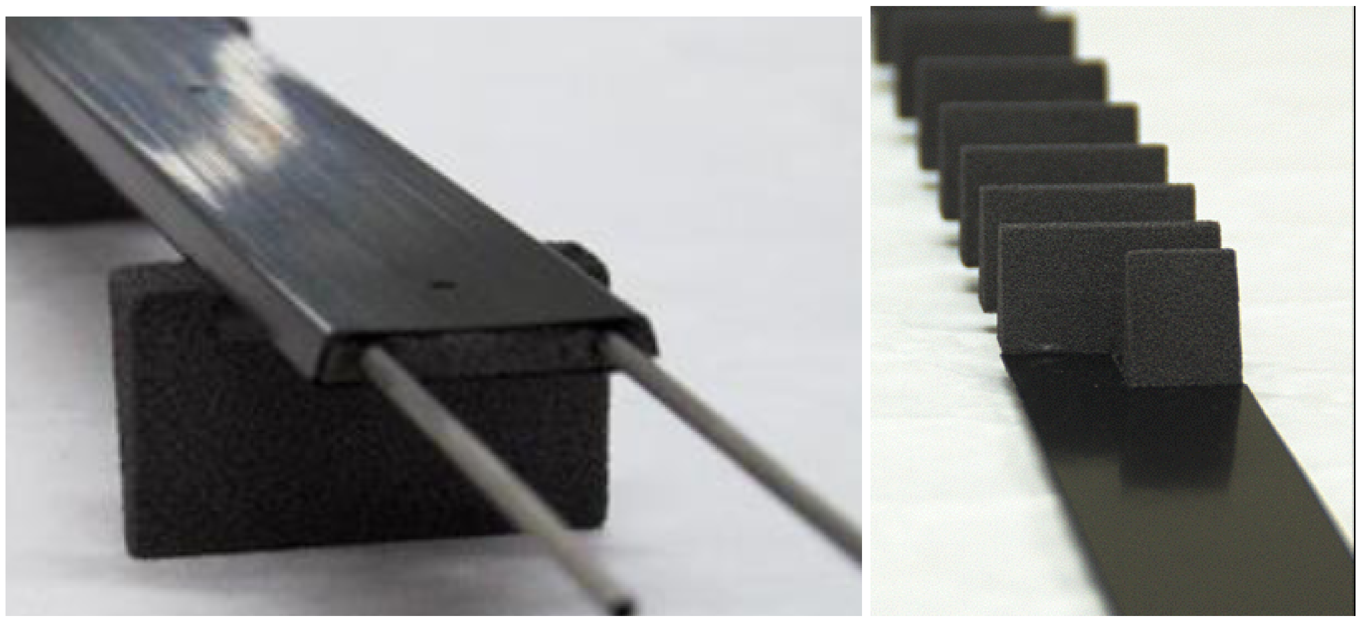
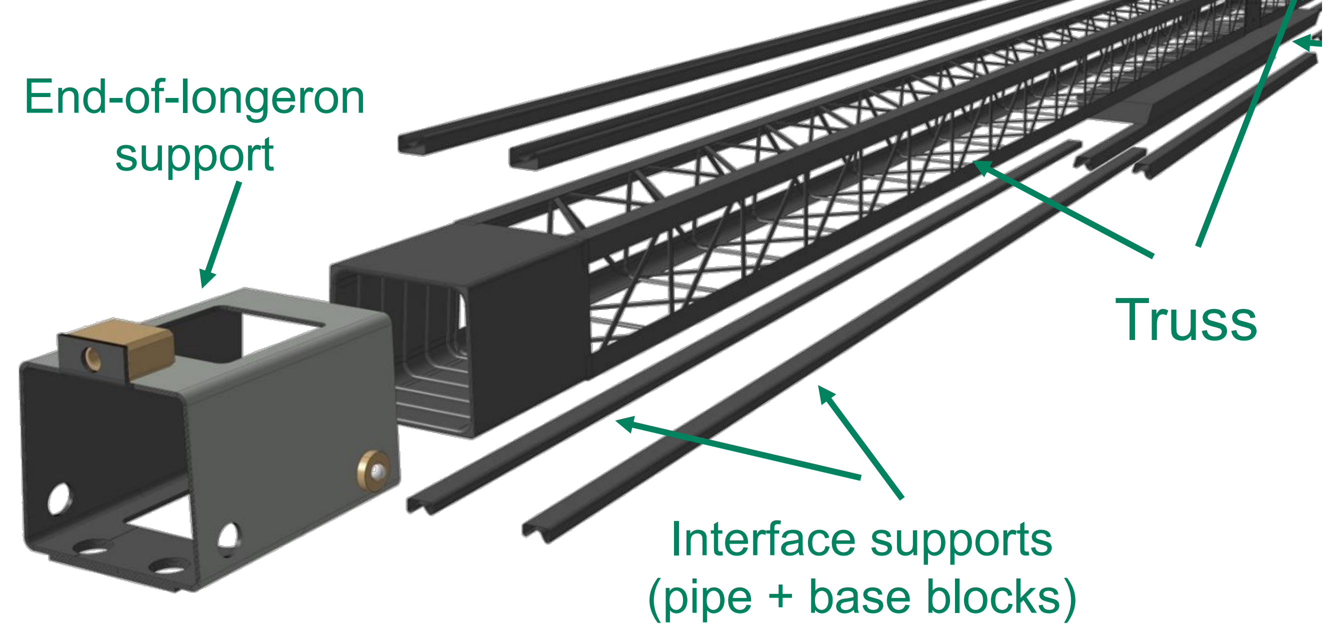
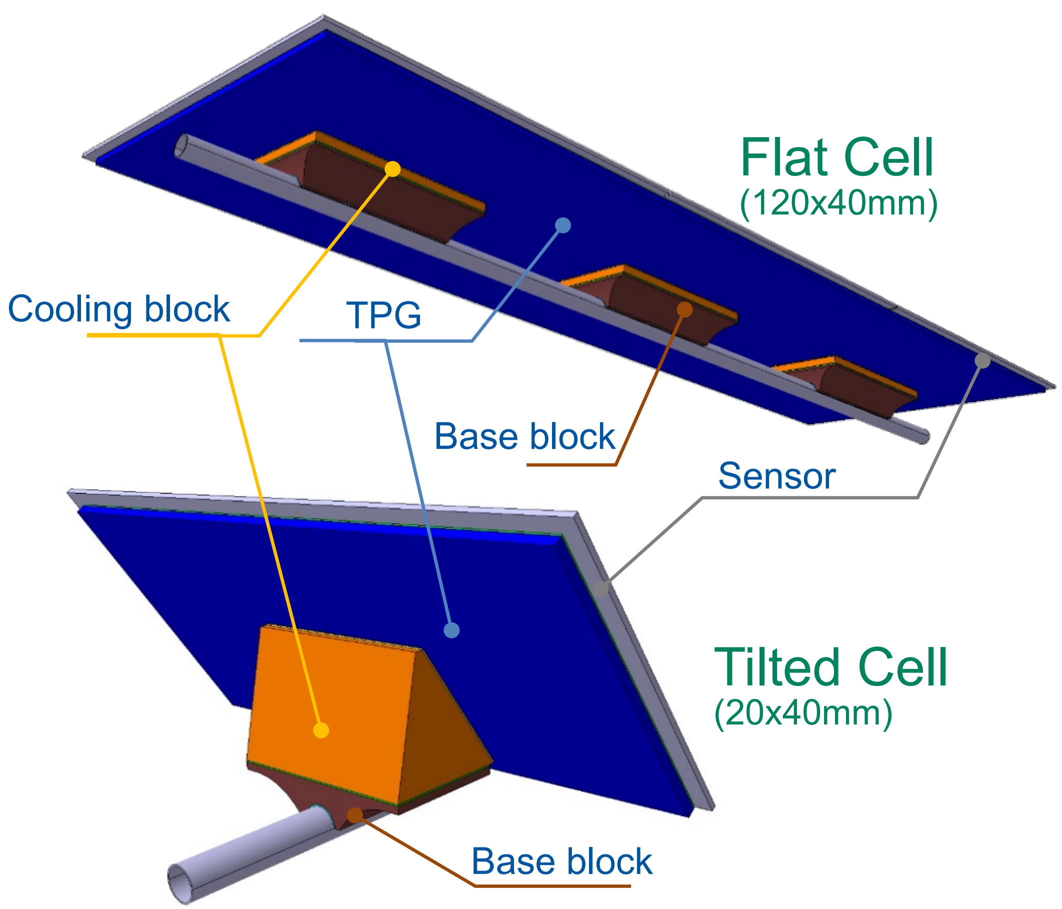


Figure 15.19: ALPINE design for the inclined layout.

- 2 x TRUSS + Central sandwich step
- CFRP interface supports
- 2 x end-of-longeron supports





Layer	TFM ($K \cdot cm^2 \cdot W^{-1}$)		
	Conductive	Convective	Global
0	11	4.3	**15**
1	16	8.6	**25**
2	12	8.6	**21**
3	15	8.6	**24**
4	18	8.6	**27**

D. GIUGNI

RAL and Liverpool

Conclusions

Physics | Lancaster University

A Higgs factory offers exciting physics potential.

Vertex and tracking detectors play an important role.

There are lots of detector developments going on worldwide, in particular CLIC has spawned a lot of R&D. **Many developments I have not been able to cover** (hybrid detectors, MIMOSA and derivatives with full frame readout, SoI, ARCADIA, Monopix, **MALTA**….)

The UK has a strong position in various areas.

TJ 65nm with ultra-thin stitched sensors are an exciting opportunity for a high resolution low mass vertex detector. Share the development (cost) with many countries and experiments: usage in **ALICE, EIC, Higgs factory**….

UK (RAL) was instrumental in launching modern MAPS!

ALPIDE is a good and available (back-up) choice for a vertex detector, especially when combined with a fast tracking detector.

ATLASPix is a good starting point for a (fast) tracking detector with a large user and development base (in the UK), available now for large tracking detector development.

It is **evolving** for a Higgs factory.

Long standing R&D projects and new experiences with low mass detectors (**Mu3e, PLUME, ZMD**….)